



Allwinner H6 V200 Datasheet

Quad-Core OTT Box Processor

Revision 1.1

Oct.17, 2017

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Revision History

Revision	Date	Description
1.0	Sep.05,2017	Initial Release Version
1.1	Oct.17,2017	1. Update the standard of ESD 2. Update the feature of Video Decoder in chapter 2.6.1. 3. Update the Oscillator Electrical Characteristics in Table 5-4 and Table 5-5. 4. Update the Package Thermal Characteristics in chapter 5.8. 5. Update the Power-on and Power-down sequence in chapter 5.7.

Contents

Declaration.....	2
Revision History.....	3
Contents.....	4
Figures.....	7
Tables.....	8
About This Documentation.....	9
1. Overview.....	10
2. Features.....	11
2.1. CPU Architecture.....	11
2.2. GPU Architecture.....	11
2.3. Memory Subsystem.....	11
2.3.1. Boot ROM.....	11
2.3.2. SDRAM.....	12
2.3.3. NAND Flash.....	12
2.3.4. SMHC.....	12
2.4. System Peripheral.....	13
2.4.1. Timer.....	13
2.4.2. GIC.....	13
2.4.3. DMA.....	14
2.4.4. CCU.....	14
2.4.5. IOMMU.....	14
2.4.6. PWM.....	14
2.4.7. Thermal Sensor.....	15
2.4.8. Message Box.....	15
2.4.9. Spinlock.....	15
2.4.10. Crypto Engine(CE).....	15
2.4.11. Embedded Crypto Engine(EMCE).....	16
2.4.12. Security ID(SID).....	16
2.4.13. CPU Configuration.....	16
2.5. Display Subsystem.....	16
2.5.1. DE3.0.....	16
2.5.2. Display Output.....	17
2.6. Video Engine.....	17
2.6.1. Video Decoder.....	17
2.6.2. Video Encoder.....	18
2.7. Image Subsystem.....	18
2.7.1. CSI.....	18
2.8. Audio Subsystem.....	18
2.8.1. Audio Hub.....	18
2.8.2. I2S/PCM.....	19

2.8.3. One Wire Audio(OWA)	19
2.8.4. DMIC.....	19
2.8.5. Audio Codec	20
2.9. Security Processing.....	20
2.10. External Peripherals	20
2.10.1. USB	20
2.10.2. UART.....	21
2.10.3. SPI.....	21
2.10.4. TWI	22
2.10.5. TSC.....	22
2.10.6. SCR	22
2.10.7. EMAC.....	23
2.10.8. EPHY	23
2.10.9. PCIe	23
2.10.10. CIR Transmitter.....	23
2.10.11. CIR Receiver.....	24
2.10.12. One Wire	24
2.11. Package	24
3. Block Diagram.....	25
4. Pin Description	26
4.1. Pin Characteristics	26
4.2. Signal Descriptions	44
5. Electrical Characteristics.....	52
5.1. Absolute Maximum Ratings	52
5.2. Recommended Operating Conditions	53
5.3. DC Electrical Characteristics	54
5.4. Oscillator Electrical Characteristics	55
5.5. External Memory AC Electrical Characteristics	56
5.5.1. Nand Flash AC Electrical Characteristics	56
5.5.2. SMHC AC Electrical Characteristics	60
5.6. External Peripheral AC Electrical Characteristics.....	62
5.6.1. LCD AC Electrical Characteristics	62
5.6.2. CSI AC Electrical Characteristics	64
5.6.3. EMAC AC Electrical Characteristics.....	65
5.6.4. CIR Receiver AC Electrical Characteristics	67
5.6.5. SPI AC Electrical Characteristics	67
5.6.6. UART AC Electrical Characteristics	68
5.6.7. TWI AC Electrical Characteristics.....	69
5.6.8. TSC AC Electrical Characteristics	70
5.6.9. SCR AC Electrical Characteristics	71
5.6.10. I2S/PCM AC Electrical Characteristics	72
5.6.11. DMIC AC Electrical Characteristics	73
5.6.12. OWA AC Electrical Characteristics	74
5.7. Power-up and Power-down Sequence	74
5.8. Package Thermal Characteristics.....	76
Appendix	78

Pin Map	78
Package Dimension	79

Figures

Figure 3-1. H6 V200 Block Diagram.....	25
Figure 5-1. Conventional Serial Access Cycle Timing (SAM0)	56
Figure 5-2. EDO Type Serial Access after Read Cycle Timing (SAM1)	56
Figure 5-3. Extending EDO Type Serial Access Mode Timing (SAM2)	57
Figure 5-4. Command Latch Cycle Timing.....	57
Figure 5-5. Address Latch Cycle Timing.....	57
Figure 5-6. Write Data to Flash Cycle Timing.....	58
Figure 5-7. Waiting R/B# Ready Timing	58
Figure 5-8. WE# High to RE# Low Timing	58
Figure 5-9. RE# High to WE# Low Timing	59
Figure 5-10. Address to Data Loading Timing	59
Figure 5-11. SMHC Output Timing Diagram in HS-SDR Mode	60
Figure 5-12. SMHC Input Timing Diagram in HS-SDR Mode	60
Figure 5-13. HV_IF Interface Vertical Timing	62
Figure 5-14. HV Interface Parallel Mode Horizontal Timing	63
Figure 5-15. Data Sample Timing	64
Figure 5-16. RGMII Interface Transmit Timing.....	65
Figure 5-17. RGMII Interface Receive Timing.....	65
Figure 5-18. RMII Interface Transmit Timing	66
Figure 5-19. RMII Interface Receive Timing	66
Figure 5-20. CIR Receiver Timing	67
Figure 5-21. SPI MOSI Timing.....	67
Figure 5-22. SPI MISO Timing.....	67
Figure 5-23. UART RX Timing	68
Figure 5-24. UART nCTS Timing.....	68
Figure 5-25. UART nRTS Timing.....	69
Figure 5-26. TWI Timing	69
Figure 5-27. TSC Data and Clock Timing.....	70
Figure 5-28. SCR Cold Reset Timing	71
Figure 5-29. SCR Warm Reset Timing.....	71
Figure 5-30. I2S/PCM Timing in Master Mode.....	72
Figure 5-31. I2S/PCM Timing in Slave Mode	73
Figure 5-32. DMIC Timing	73
Figure 5-33. OWA Timing.....	74
Figure 5-34. Power On Sequence.....	75
Figure 5-35. H6 V200 Power Down Sequence	76

Tables

Table 4-1. Pin Characteristics	27
Table 4-2. Signal Descriptions	44
Table 5-1. Absolute Maximum Ratings	52
Table 5-2. Recommended Operating Conditions	53
Table 5-3. DC Electrical Characteristics	54
Table 5-4. 24MHz Crystal Characteristics	55
Table 5-5. 32768Hz Crystal Characteristics	55
Table 5-6. NAND Timing Constants	59
Table 5-7. SMHC Timing Constants	60
Table 5-8. LCD HV_IF Interface Timing Constants	63
Table 5-9. CSI Interface Timing Constants	64
Table 5-10. RGMII Transmit Timing Constants	65
Table 5-11. RGMII Interface Receive Timing Constants	65
Table 5-12. RMII Interface Transmit Timing Constants	66
Table 5-13. RMII Interface Receive Timing Constants	66
Table 5-14. CIR Receiver Timing Constants	67
Table 5-15. SPI Timing Constants	68
Table 5-16. UART Timing Constants	69
Table 5-17. TWI Timing Constants	69
Table 5-18. TSC Timing Constants	70
Table 5-19. SCR Timing Constants	71
Table 5-20. I2S/PCM Timing Constants in Master Mode	72
Table 5-21. I2S/PCM Timing Constants in Slave Mode	73
Table 5-22. DMIC Timing Constants	73
Table 5-23. OWA Timing Constants	74
Table 5-24. H6 V200 Thermal Resistance Characteristics	77

About This Documentation

The documentation describes features of each module, pin/signal characteristics, PLL electrical characteristics, the interface timing, thermal and package of H6 V200 processor. For details about register descriptions of each module, see the *H6 V200 User Manual*.

Intended Audience

The document is intended for:

- Hardware designers for electronics
- Sales personnel for electronic parts and components

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 WARNING	A warning means that injury or death is possible if the instructions are not obeyed.
 CAUTION	A caution means that damage to equipment is possible.
 NOTE	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

1. Overview

The Allwinner H6 V200 is a highly cost-efficient quad-core OTT Box processor, which is a part of growing home entertainment products that offer high-performance processing with a high degree of functional integration.

The H6 V200 processor has some very exciting features, for example:

- **CPU:** Quad-core ARM Cortex™-A53 Processor, a power-efficient ARM v8 architecture, it has 64 and 32bit execution states for scalable high performance ,which includes a NEON multimedia processing engine.
- **Graphics:** Mali-T720 Multi-Core, proven Midgard architecture with two shade cores, provides users with superior experience in video playback and mainstream game; OpenGL ES3.1and OpenCL1.2 standards are supported.
- **Video Engine:** H6 V200 provides multi-format high-definition video encoder/decoder with dedicated hardware, including H.265 decoder by 4K@60fps, H.264 decoder by 4K@30fps, H.263 decoder by 1080p@60fps, VP9 decoder by 4K@30fps, MPEG1/2/4 decoder by 1080p@60fps, VC1/VP8/AVS/AVS+ jizhun decoder by 1080p@60fps, H.264 encoder by 1080p@60fps.
- **Display Subsystem:** Supports Allwinner's SmartColor 3.0 for excellent display experience, and three display interfaces including RGB LCD display for LCD, HDMI2.0a output and TVOUT(Controlled by ATE) for TV.
- **Audio Subsystem:** Supports popular digital audio interfaces such as I2S/PCM, OWA, DMIC and Audio Hub, and supports I2S/PCM for connecting to an external audio codec. To reduce total system cost and enhance high integration, the H6 V200 processor also integrates an audio codec(Controlled by ATE).
- **Memory Controller:** The processor supports many types of external memory devices, including DDR4/DDR3/DDR3L/LPDDR2/LPDDR3, NAND Flash with full disk encryption , Nor Flash, SD/SDIO/MMC including eMMC up to rev5.1.
- **Security System:** The processor delivers hardware security features that enable trustzone security system, Digital Rights Management(DRM) , information encryption/decryption, secure boot and secure efuse.
- **Interfaces:** The processor has a broad range of hardware interfaces such as parallel CMOS sensor interface, 10/100/1000Mbps EMAC with EPHY(Controlled by ATE), USB OTG v2.0 operating at high speed(480Mbps) with PHY, USB3.0/2.0 Host with PHY, and a variety of other popular interfaces(SPI,UART,PCIe,One Wire,CIR,TSC,TWI,SCR).

2. Features

2.1. CPU Architecture

- Quad-core ARM Cortex™-A53 Processor
- Power-efficient ARM v8 architecture
- 64 and 32bit execution states for scalable high performance
- Trustzone technology supported
- 3~10x better software encryption performance
- Supports NEON Advanced SIMD(Single Instruction Multiple Data)instruction for acceleration of media and signal processing functions
- Supports Large Physical Address Extensions(LPAE)
- VFPv4 Floating Point Unit
- 32KB L1 Instruction cache and 32KB L1 Data cache per core
- 512KB L2 cache shared

2.2. GPU Architecture

- Mali-T720 Multi-Core, proven Midgard architecture with two shade cores
- Supports OpenGL ES 3.1/3.0/2.0/1.1, OpenCL 1.2/1.1, DirectX 11 FL9_3, and Renderscript/Filterscript
- Supports Transaction Elimination, saving external bandwidth and energy
- Supports ASTC, best-in-class compression, reduced size and improved quality
- Supports FAST(4x)FSAA, IO Coherency

2.3. Memory Subsystem

2.3.1. Boot ROM

- Supports system boot from the following devices:
 - NAND Flash
 - SD card
 - eMMC
 - SPI Nor Flash
- Supports secure boot and normal boot
- Supports one key USB mass production upgrade
- Supports system code download through USB OTG and card
- Supports boot media priority sequence through boot select pin and efuse

2.3.2. SDRAM

- Compatible with JEDEC standard DDR4/DDR3/DDR3L/LPDDR2/LPDDR3 SDRAM
- Supports clock frequency up to 933MHz(DDR4)
- 32-bit bus width
- Up to 2GB address space
- Supports 2 chip selects
- 18 address signal lines and 3 bank signal lines
- Random read or write operation is supported

2.3.3. NAND Flash

- Up to 8-bit data bus width
- Up to 80-bit ECC per 1024 bytes
- Supports 2CE/2RB
- Supports 1024, 2048, 4096, 8192, 16384, 32768 bytes size per page
- Supports SLC/MLC/TLC flash and EF-NAND memory
- Supports SDR, ONFI DDR and Toggle DDR NAND
- Supports full disk encryption(FDE) function
- Embedded DMA to do data transfer
- Supports data transfer together with normal DMA

2.3.4. SMHC

- Up to 3 SD/MMC host controller(SMHC) interfaces
- SMHC0 controls the device that comply with the Secure Digital Memory(SD3.0)
 - 4-bit bus width
 - SDR mode 50MHz@3.3V IO pad
- SMHC1 controls the devices that comply with the Secure Digital Input/Output(SDIO3.0)
 - 4-bit bus width
 - SDR mode 50MHz@3.3V IO pad
 - SDR mode 150MHz@1.8V IO pad
 - DDR mode 50MHz@1.8V IO pad
- SMHC2 controls the devices that comply with the MultiMediaCard(MMC5.1)
 - 8-bit bus width
 - SDR mode 150MHz@1.8V IO pad
 - DDR mode 100MHz@1.8V IO pad
 - DDR mode 50MHz@3.3V IO pad
- SMHC2 supports full disk encryption(FDE) function
- Supports hardware CRC generation and error detection
- Supports block size of 1 to 65535 bytes

2.4. System Peripheral

2.4.1. Timer

- The timer module implements the timing and counting functions, which includes Timer0 and Timer1, Watchdog, AVS and 64-bit counter
- Timer0 and Timer1 for system scheduler counting
 - Configurable 8 prescale factor
 - Programmable 32-bit down timer
 - Supports two working modes: continue mode and single count mode
 - Generates an interrupt when the count is decreased to 0
- 1 Watchdog for transmitting a reset signal to reset the entire system after an exception occurs in the system
 - Supports 12 initial values to configure
 - Supports the generation of timeout interrupts
 - Supports the generation of reset signal
 - Supports watchdog restart the timing
- 2 AVS counters(AVS0 and AVS1) for synchronizing video and audio in the player
 - Programmable 33-bit up timer
 - Initial value can be updated anytime
 - 12-bit frequency divider factor
 - Supports Pause/Start function
- One 64-bit Counter to count timing for GPU
 - Supports clear zero function
 - Performs latch operation once before getting the current counter value

2.4.2. GIC

- Supports 16 Software Generated Interrupts(SGIs), 16 Private Peripheral Interrupts(PPIs) and 147 Shared Peripheral Interrupts(SPIs)
- Enabling, disabling, and generating processor interrupts from hardware interrupt
- Interrupt masking and prioritization
- Uniprocessor and multiprocessor environments
- The ARM architecture Security Extensions
- The ARM architecture Virtualization Extensions
- Wakeup events in power-management environments

2.4.3. DMA

- Up to 16-channel DMA
- Interrupt generated for each DMA channel
- Transfers data width of 8/16/32/64-bit
- Supports linear and IO address modes
- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory, peripheral-to-peripheral
- Supports transfer with linked list
- DRQ response includes wait mode and handshake mode
- DMA channel supports pause function

2.4.4. CCU

- 11 PLLs
- Supports an external 32KHz crystal oscillator ,an external 24MHz DCXO and an internal RC16MHz oscillator
- Supports clock configuration and clock generated for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

2.4.5. IOMMU

- Supports virtual address to physical address mapping by hardware implementation
- Supports DE0/2, VE_R, VE, CSI, VP9 parallel address mapping
- Supports DE0/2, VE_R, VE, CSI, VP9 bypass function independently
- Supports DE0/2,VE_R,VE,CSI,VP9 prefetch independently
- Supports DE0/2,VE_R,VE,CSI,VP9 Interrupt handing mechanism independently
- Supports level1 and level2 TLB for special using, and level2 TLB for sharing
- Supports TLB Fully cleared and Partially disabled
- Supports trigger PTW behavior when TLB miss
- Supports checking the permission
- Performance: Average (L1+L2)TLB Hit rate: up to 99.9%, Average Latency: 5±1cycle

2.4.6. PWM

- Supports outputting two kinds of waveform: continuous waveform and pulse waveform
- 0% to 100% adjustable duty cycle
- Up to 24MHz output frequency
- The minimum resolution is $1/65536$

2.4.7. Thermal Sensor

- Temperature Accuracy: $\pm 3^{\circ}\text{C}$ from 0°C to $+100^{\circ}\text{C}$, $\pm 5^{\circ}\text{C}$ from -20°C to $+125^{\circ}\text{C}$
- Power supply voltage: 1.8V
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Supports 2 sensors: sensor0 for CPU, sensor1 for GPU

2.4.8. Message Box

- Provides interrupt communication mechanism for on-chip processor
- Two users for Message Box: user0 for CPU, user1 for GPU
- Each of Queue has a 4x32-bits FIFO for eight Message Queues
- Each of Queue could be configured as transmitter or receiver

2.4.9. Spinlock

- 32 spinlocks
- Two kinds of status of lock register: TAKEN and NOT TAKEN
- Lock time of the processor is predictable (less than 200 cycles)

2.4.10. Crypto Engine(CE)

- Supports Symmetrical algorithm: AES, DES, TDES, XTS
 - Supports ECB, CBC, CTS, CTR, CFB, OFB, CBC-MAC mode for AES
 - Supports 128/192/256-bit key for AES
 - Supports ECB, CBC, CTR, CBC-MAC mode for DES/TDES
 - Supports 256/512-bit key for XTS
- Supports Hash algorithm: MD5, SHA, HMAC
 - Supports SHA1, SHA224, SHA384, SHA512 for SHA
 - Supports HMAC-SHA1, HMAC-SHA256 for HMAC
 - MD5, SHA, HMAC are padded using hardware. If not last package, input should align with 512 bits
- Supports Asymmetrical algorithm: RSA, ECC
 - RSA supports 512/1024/2048/4096-bit width
 - ECC Supports 160/224/256/384/521-bit width
- Supports 160-bit hardware PRNG with 175-bit seed
- Supports 256-bit hardware TRNG
- Internal Embedded DMA to do data transfer
- Supports secure and non-secure interfaces respectively

- Supports task chain mode for each request. Task or task chain are executed at request order
- 8 scatter group(sg) are supported for both input and output data
- DMA has multiple channel, each corresponding to one suit of algorithms

2.4.11. Embedded Crypto Engine(EMCE)

- Connects directly to SMHC or NDFC for disc encryption application
- Supports AES algorithm
- Supports 128-bit, 192-bit and 256-bit key size for AES
- Supports ECB, CBC, XTS modes

2.4.12. Security ID(SID)

- Supports 4K-bit EFUSE for chip ID and security application

2.4.13. CPU Configuration

- Capable of CPU reset, including core reset, debug circuit reset, etc
- Capable of other CPU-related control, including interface control, CP15 control, and power control, etc
- Capable of checking CPU status, including idle status, SMP status, and interrupt status, etc

2.5. Display Subsystem

2.5.1. DE3.0

- Output size up to 4096x4096
- Supports four alpha blending channels for main display, two channels for aux display
- Supports four overlay layers in each channel, and has an independent scaler
- Supports potter-duff compatible blending operation
- Supports input format semi-planar of YUV422/YUV420/YUV411/P010/P210 and planar of YUV422/YUV420/YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565
- Supports Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-side Half 3D format data
- Supports 10-bit processing path for HDR video
- Supports HDR-to-SDR and HLG-to-HDR conversion for HDR video and SDR-to-HDR conversion for SDR UI
- Supports SmartColor 3.0 for excellent display experience
 - Supports high quality video scaler with edge pattern detection
 - Adaptive detail/edge enhancement

- Adaptive color enhancement
- Adaptive contrast enhancement and fresh tone rectify
- Adaptive de-noising with image quality assessment and block detector function
- Supports 3-D de-interlacer with low angle interpolation
- Supports writeback for high efficient dual display and miracast

2.5.2. Display Output

- Supports HDMI2.0a output
 - Up to 4K@60fps resolution
 - Compatible with HDCP 2.2 for HDMI
 - Integrated CEC hardware
 - Supports HDMI and LCD display output at the same time
 - Supports HDMI 3D display
 - Supports 8/10-bit color depth
 - Supports HDCP1.4
 - Supports output format: RGB, YUV444, YUV422, YUV420
 - Supports HDR
- Supports TV Encoder
 - System resources are controlled by ATE
 - Supports CCIR656 and Serial YUV interface
 - 1 CVBS out, supports NTSC and PAL
 - Plug status auto detecting
- Supports RGB LCD interface with DE/SYNC mode
 - Up to 1920x1080@60fps resolution
 - 18-bit data bus
 - Supports RGB666/RGB656 dither function

2.6. Video Engine

2.6.1. Video Decoder

- Supports multi-format video playback, including:
 - H.265 Main10/L5.1 : 4K@60fps
 - H.264 BP/MP/HP Level4.2 : 4K@30fps
 - H.263 BP : 1080p@60fps
 - MPEG1 MP/HL : 1080p@60fps
 - MPEG2 MP/HL : 1080p@60fps
 - MPEG4 SP/ASP L5 : 1080p@60fps
 - Sorenson Spark : 1080p@60fps
 - VP8 N/A : 1080p@60fps

- VP9 Profile 0/2 4K@30fps
- VC1 SP/MP/AP : 1080p@60fps
- AVS-P2/AVS-P16(AVS+) jizhun : 1080p@60fps
- Xvid N/A : 1080p@60fps
- Supports 1080p blu-ray 3D
- Supports 3D size:3840x1080,1920x2160
- Supports decoding output format: T32 x 32, YV12, NV12, NV21, and HEVC also supports afbc

2.6.2. Video Encoder

- Supports H.264 BP/MP/HP video encoder up to 1080p@60fps
- Supports JPEG@4080x4080 video encoder
- Supports input picture size up to 4800x4800
- Supports input format: tiled (128x32)/YU12/YV12/NU12/NV12/ARGB/YUYV
- Supports Alpha blending
- Supports thumb generation
- Supports 4x2 scaling ratio: from 1/16 to 64 arbitrary non-integer ratio
- Supports rotated input

2.7. Image Subsystem

2.7.1. CSI

- Supports 8/10bit digital camera interface
- Supports BT656 interface
- Supports ITU-R BT.656 time-multiplexed format
- Maximum still capture resolution for parallel interface to 5M
- Maximum video capture resolution for parallel interface to 1080p@30fps
- Maximum pixel clock for parallel to 148.5MHz

2.8. Audio Subsystem

2.8.1. Audio Hub

- Concurrent switching between audio clients
 - The audio clients are I2S/PCM, DAM and APBIF
 - A TX client can talk to multiple RX clients simultaneously
 - A RX client can only talk to one TX clients

- Scalable MxN crossbar switch, where
 - M is the number of TX clients
 - N is the number of RX clients
- Supports three 64x32bit TX streams FIFO and three 128x32bit RX streams FIFO for APB DMA operations
- Supports two DAM(Digital Audio Mixer) interface, one I2S/PCM interface for HDMI ,one I2S/PCM interface for Audio Codec

2.8.2. I2S/PCM

- Up to 4 I2S/PCM controllers
- One controller for HDMI, one controller for Audio Codec,others for digital audio mixer application
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
- Compliant with Left-justified, Right-justified, PCM mode, and TDM (Time Division Multiplexing) format
- Supports full-duplex synchronous work mode
- Supports Master/Slave mode
- Supports clock up to 24.576MHz
- Supports adjustable audio sample resolution from 8-bit to 32-bit
- Supports 8-bit u-law and 8-bit A-law companded sample
- One 128 depth x 32-bit width TXFIFO for data transmit, one 64 depth x 32-bit width RXFIFO for data receive
- Supports programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Programmable FIFO thresholds

2.8.3. One Wire Audio(OWA)

- IEC-60958 transmitter and receiver functionality
- Compatible with S/PDIF interface
- Supports channel status insertion for the transmitter
- Supports channel status capture on the receiver
- Hardware Parity generation on the transmitter
- Hardware Parity checking on the receiver
- One 128 x 24 bits TX FIFO and one 64 x 24 bits RXFIFO for audio data transfer
- Programmable FIFO thresholds
- Supports 16-bit,20-bit and 24-bit data formats

2.8.4. DMIC

- Up to 8 channels
- Supports maximum 8 digital microphones
- Supports sample rate from 8kHz to 48kHz

2.8.5. Audio Codec

- System resources are controlled by ATE
- Two audio digital-to-analog(DAC) channels
 - 100dB SNR@A-weight
 - Supports DAC Sample Rates from 8kHz to 192kHz
- Supports analog/digital volume control
- Two differential microphone inputs
- One lineout output with voltage ramp
- Two audio analog-to-digital(ADC) channels
 - 92dB SNR@A-weight
 - Supports ADC Sample Rates from 8kHz to 48kHz
- Supports Automatic Gain Control(AGC) adjusting the ADC recording output

2.9. Security Processing

- Full Disk Encryption(FDE), supports AES-ECB/CBC
- 4K bits Efuse(OTP)
- Protection for JTAG and other debugging port
- HDCP 2.2/1.4 protection for HDMI outputs
- Trusted execution environment(TEE)
- Digital rights management(DRM)
- Mainstream advanced CA
- Secure boot
- Secure Storage
- Secure upgrade
- Transparent RAM scrambling
- Hardware TRNG

2.10. External Peripherals

2.10.1. USB

- One USB 2.0 OTG
 - Complies with USB2.0 Specification
 - Supports High-Speed (HS,480 Mbps),Full-Speed(FS,12 Mbps) and Low-Speed(LS,1.5 Mbps) in host mode
 - Supports High-Speed (HS,480 Mbps),Full-Speed(FS,12 Mbps) in device mode
 - Complies with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a for host mode
 - Up to 8 User-Configurable Endpoints for Bulk, Isochronous and Interrupt bi-directional transfers (Endpoint1, Endpoint2, Endpoint3, Endpoint4)

- Supports (4KB+64Bytes) FIFO for EPs(including EP0)
- Supports point-to-point and point-to-multipoint transfer in both host and peripheral mode
- One USB 2.0 Host
 - Supports High-Speed (HS,480 Mbps),Full-Speed(FS,12 Mbps) and Low-Speed(LS,1.5 Mbps) device
 - Compatible with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a.
- One USB 3.0 Host
 - Supports Super-Speed(SS,5 Gbps),High-Speed (HS,480 Mbps),Full-Speed(FS,12 Mbps) and Low-Speed(LS,1.5 Mbps) in host mode
 - USB3.0 PIPE3 PHY interface
 - USB 2.0 UTMI+(L3) PHY interface
 - Simultaneous IN and OUT transfer support in superspeed mode

2.10.2. UART

- Up to 5 UART controllers
- Two of 5 UART controllers support 2-wire while others support 4-wire
- Compatible with industry-standard 16550 UARTs
- 256-Bytes Transmit and Receive data FIFOs
- Capable of speed up to 5Mbps
- Supports 5-8 data bits and 1/1.5/2 stop bits
- Supports Even, Odd or No Parity
- Supports DMA controller interface
- Supports Software/ Hardware Flow Control
- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode

2.10.3. SPI

- Up to 2 SPI controllers
- Full-duplex synchronous serial interface
- 5 clock sources
- Master/Slave configurable
- Four chip selects to support multiple peripherals
- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- Interrupt or DMA support
- Supports 3-Wire/4-Wire SPI
- Supports programmable serial data frame length: 0-bit to 32-bit
- Supports Standard SPI,Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI

2.10.4. TWI

- Up to 4 TWI(Two Wire Interface) controllers
- Software-programmable for slave or master
- Supports repeated START signal
- Allows 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports speed up to 400 kbit/s ('fast mode')
- Allows operation from a wide range of input clock frequency

2.10.5. TSC

- Up to 4 TS controllers
- Supports SPI/SSI interface, interface timing parameters are configurable
- 32 channels PID filter for each TSF
- Multiple transport stream packet (188, 192, 204) format support
- Hardware packet synchronous byte error detecting
- Hardware PCR packet detecting
- 64x16-bit FIFO for TSG, 64x32-bit FIFO for TSF
- Configurable SPI transport stream generator for streams in DRAM memory
- Supports DVB-CSA V1.1, DVB-CSA V2.1 Descrambler

2.10.6. SCR

- Up to 2 SCR(Smart Card Reader) controllers
- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Supports asynchronous half-duplex character transmission and block transmission
- Supports synchronous and any other non-ISO 7816 and non-EMV cards
- Performs functions needed for complete smart card sessions, including:
 - Card activation and deactivation
 - Cold/warm reset
 - Answer to Reset (ATR) response reception
 - Data transfers to and from the card

2.10.7. EMAC

- Compliant with the IEEE 802.3-2002 standard
- Supports 10/100/1000-Mbps data transfer rates
- Supports RMII/RGMII PHY interface
- Supports a variety of flexible address filtering modes
- Supports full and half duplex operations
- Programmable frame length to support Standard or Jumbo Ethernet frames with size up to 16KB
- Supports linked-list descriptor list structure
- 4KB TXFIFO for transmission packets and 16KB RXFIFO for reception packets

2.10.8. EPHY

- System resources are controlled by ATE
- Fully IEEE 802.3 10/100 Base-TX compliant and supports EEE
- Auto negotiation and parallel detection capability for automatic speed and duplex selection
- Programmable loopback mode for diagnostic
- Supports WOL (Wake-On-Lan) functionality
- Design for Testability with extensive testability feature and 95% fault coverage
- Power consumption (100Base-TX) less than 140mW

2.10.9. PCIe

- Complies with PCI Express Base 2.0 Specification
- Embedded PCI Express PHY, supports x1 Gen2(5.0 Gbps) lane
- Only supports Root Complex(RC) mode
- Maximum payload size: 256 bytes
- Supports 2 Inbound windows and 2 Outbound windows

2.10.10. CIR Transmitter

- Supports arbitrary wave generator
- Configurable carrier frequency
- 128 bytes FIFO for data buffer
- Interrupt and DMA supported

2.10.11. CIR Receiver

- Flexible receiver for consumer IR remote control
- Programmable FIFO thresholds
- 64x8 bits FIFO for data buffer
- Sample clock up to 1MHz

2.10.12. One Wire

- Hardware implement of 1-wire protocol
- Supports master function
- Supports simple mode and standard mode

2.11. Package

- FBGA 451 balls, 0.65mm ball pitch, 15mm x 15mm

3. Block Diagram

Figure 3-1 shows the block diagram of H6 V200 processor.

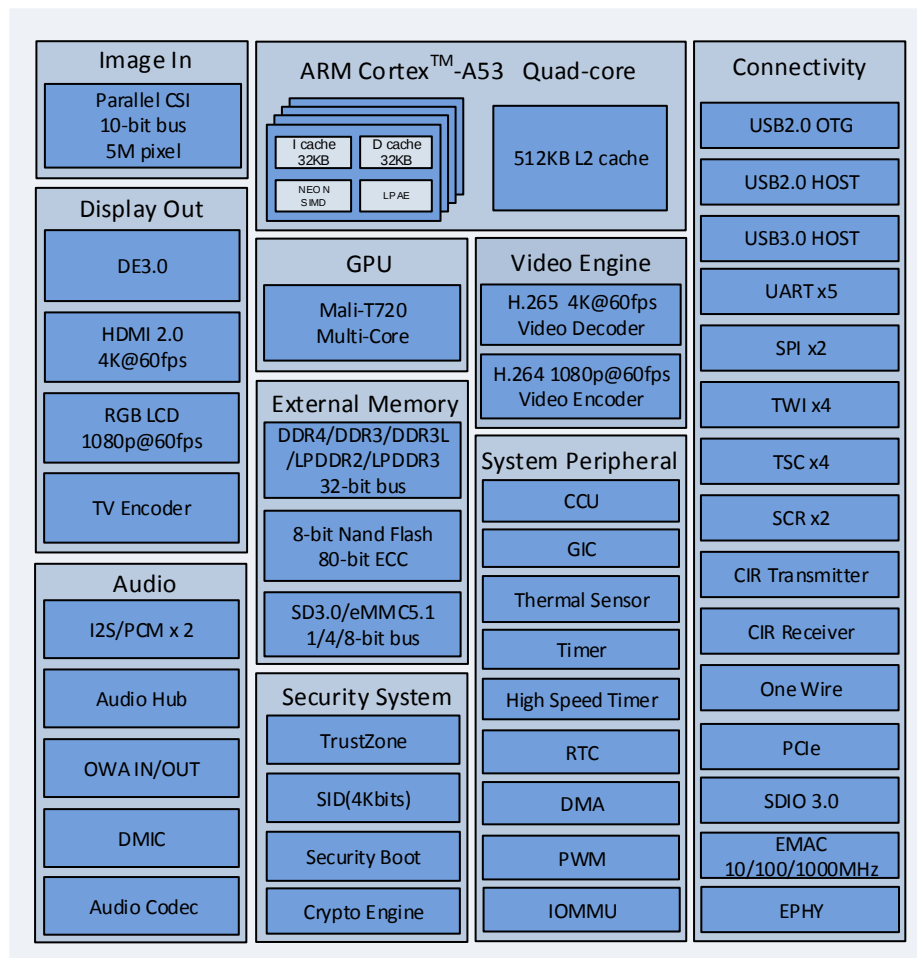


Figure 3-1. H6 V200 Block Diagram

4. Pin Description

4.1. Pin Characteristics

Table 4-1 lists the characteristics of H6 V200 Pins from seven aspects: BALL#, Pin Name, Default Function, Type, Reset State, Default Pull Up/Down, and Buffer Strength.

- (1).**Ball#**: Package ball numbers associated with each signals.
- (2).**Pin Name**: The name of the package pin.
- (3).**Signal Name**: The signal name for that pin in the mode being used.
- (4).**Function**: Multiplexing function number.
- (5).**Ball Reset Rel. Function**: The function is automatically configured after RESET from low to high.
- (6).**Type**: Denotes the signal direction
 - I (Input),
 - O (Output),
 - I/O(Input / Output),
 - OD(Open-Drain),
 - A (Analog),
 - AI(Analog Input),
 - AO(Analog Output),
 - A I/O(Analog Input/Output),
 - P (Power),
 - G (Ground)
- (7).**Ball Reset State** : The state of the terminal at reset.
 - Z(High-impedance)
- (8).**Pull Up/Down** : Denotes the presence of an internal pull-up or pull-down resistor. Pull-up(PU) and Pull-down(PD) resistors can be enabled or disabled via software.
- (9).**Buffer Strength** : Defines drive strength of the associated output buffer.
- (10).**Power Supply** : The voltage supply for the terminal's IO buffers.

Table 4-1. Pin Characteristics

Ball# ⁽¹⁾	Pin Name ⁽²⁾	Signal Name ⁽³⁾	Function ⁽⁴⁾	Ball Reset Rel. Function ⁽⁵⁾	Type ⁽⁶⁾	Ball Reset State ⁽⁷⁾	Pull Up/Down ⁽⁸⁾	Buffer Strength ⁽⁹⁾ (mA)	Power Supply ⁽¹⁰⁾
DRAM									
AB18	SDQ0	SDQ0	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC17	SDQ1	SDQ1	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB17	SDQ2	SDQ2	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC16	SDQ3	SDQ3	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB15	SDQ4	SDQ4	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB14	SDQ5	SDQ5	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC14	SDQ6	SDQ6	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC13	SDQ7	SDQ7	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB19	SDQ8	SDQ8	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC20	SDQ9	SDQ9	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC21	SDQ10	SDQ10	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB20	SDQ11	SDQ11	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB23	SDQ12	SDQ12	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA23	SDQ13	SDQ13	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA22	SDQ14	SDQ14	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y22	SDQ15	SDQ15	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC6	SDQ16	SDQ16	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB6	SDQ17	SDQ17	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC7	SDQ18	SDQ18	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB7	SDQ19	SDQ19	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC9	SDQ20	SDQ20	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB9	SDQ21	SDQ21	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC10	SDQ22	SDQ22	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB10	SDQ23	SDQ23	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y1	SDQ24	SDQ24	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y2	SDQ25	SDQ25	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA1	SDQ26	SDQ26	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA2	SDQ27	SDQ27	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC2	SDQ28	SDQ28	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC3	SDQ29	SDQ1	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC4	SDQ30	SDQ30	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB4	SDQ31	SDQ31	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC15	SDQS0P	SDQS0P	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB16	SDQS0N	SDQS0N	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC22	SDQS1P	SDQS1P	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB22	SDQS1N	SDQS1N	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB8	SDQS2P	SDQS2P	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC8	SDQS2N	SDQS2N	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB1	SDQS3P	SDQS3P	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB2	SDQS3N	SDQS3N	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC18	SDQM0	SDQM0	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y23	SDQM1	SDQM1	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB11	SDQM2	SDQM2	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB5	SDQM3	SDQM3	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC12	SCKP	SCKP	NA	NA	O	Z	NA	NA	VCC-DRAM
AB12	SCKN	SCKN	NA	NA	O	Z	NA	NA	VCC-DRAM
W13	SCS0	SCS0	NA	NA	O	Z	NA	NA	VCC-DRAM
Y14	SCS1	SCS1	NA	NA	O	Z	NA	NA	VCC-DRAM
W14	SCKE0	SCKE0	NA	NA	O	Z	NA	NA	VCC-DRAM
Y11	SCKE1	SCKE1	NA	NA	O	Z	NA	NA	VCC-DRAM
AA15	SA0	SA0	NA	NA	O	Z	NA	NA	VCC-DRAM
AA17	SA1	SA1	NA	NA	O	Z	NA	NA	VCC-DRAM
AA19	SA2	SA2	NA	NA	O	Z	NA	NA	VCC-DRAM
Y20	SA3	SA3	NA	NA	O	Z	NA	NA	VCC-DRAM
Y16	SA4	SA4	NA	NA	O	Z	NA	NA	VCC-DRAM
Y10	SA5	SA5	NA	NA	O	Z	NA	NA	VCC-DRAM
Y8	SA6	SA6	NA	NA	O	Z	NA	NA	VCC-DRAM
AA5	SA7	SA7	NA	NA	O	Z	NA	NA	VCC-DRAM
AA7	SA8	SA8	NA	NA	O	Z	NA	NA	VCC-DRAM

Ball# ⁽¹⁾	Pin Name ⁽²⁾	Signal Name ⁽³⁾	Function ⁽⁴⁾	Ball Reset Rel. Function ⁽⁵⁾	Type ⁽⁶⁾	Ball Reset State ⁽⁷⁾	Pull Up/Down ⁽⁸⁾	Buffer Strength ⁽⁹⁾ (mA)	Power Supply ⁽¹⁰⁾
Y3	SA9	SA9	NA	NA	O	Z	NA	NA	VCC-DRAM
Y17	SA10	SA10	NA	NA	O	Z	NA	NA	VCC-DRAM
W17	SA11	SA11	NA	NA	O	Z	NA	NA	VCC-DRAM
W16	SA12	SA12	NA	NA	O	Z	NA	NA	VCC-DRAM
W5	SA13	SA13	NA	NA	O	Z	NA	NA	VCC-DRAM
AA14	SWE/SA14	SWE/SA14	NA	NA	O	Z	NA	NA	VCC-DRAM
W19	SCAS/SA15	SCAS/SA15	NA	NA	O	Z	NA	NA	VCC-DRAM
AA4	SRAS/SA16	SRAS/SA16	NA	NA	O	Z	NA	NA	VCC-DRAM
Y7	SA17	SA17	NA	NA	O	Z	NA	NA	VCC-DRAM
AA11	SACT	SACT	NA	NA	O	Z	NA	NA	VCC-DRAM
W4	SPAR	SPAR	NA	NA	O	Z	NA	NA	VCC-DRAM
Y21	SALERT	SALERT	NA	NA	I	Z	NA	NA	VCC-DRAM
W7	SBA0	SBA0	NA	NA	O	Z	NA	NA	VCC-DRAM
AA20	SBA1	SBA1	NA	NA	O	Z	NA	NA	VCC-DRAM
W8	SBG0	SBG0	NA	NA	O	Z	NA	NA	VCC-DRAM
W11	SBG1	SBG1	NA	NA	O	Z	NA	NA	VCC-DRAM
AA13	SODT0	SODT0	NA	NA	O	Z	NA	NA	VCC-DRAM
AA10	SODT1	SODT1	NA	NA	O	Z	NA	NA	VCC-DRAM
AA3	SRST	SRST	NA	NA	O	NA	NA	NA	VCC-DRAM
W2	SZQ	SZQ	NA	NA	AI	Z	NA	NA	VCC-DRAM
V6	SVREF	SVREF	NA	NA	P	Z	NA	NA	VCC-DRAM
U8,U13,U14,U16,V9, V10, V11, V15	VCC-DRAM	VCC-DRAM	NA	NA	P	NA	NA	NA	NA
W22	VDD18-DRAM	VDD18-DRAM	NA	NA	P	NA	NA	NA	NA
GPIO C									
R21	PC0	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_WE	2		O				
		Reserved	3		NA				
		SPIO_CLK	4		I/O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
R20	PC1	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_ALE	2		O				
		SDC2_DS	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
P22	PC2	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_CLE	2		O				
		Reserved	3		NA				
		SPIO_MOSI	4		I/O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
T20	PC3	Input	0	Function7	I	PU	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_CE0	2		O				
		Reserved	3		NA				
		SPIO_MISO	4		I/O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
N20	PC4	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_RE	2		O				
		SDC2_CLK	3		O				

Ball# ⁽¹⁾	Pin Name ⁽²⁾	Signal Name ⁽³⁾	Function ⁽⁴⁾	Ball Reset Rel. Function ⁽⁵⁾	Type ⁽⁶⁾	Ball Reset State ⁽⁷⁾	Pull Up/Down ⁽⁸⁾	Buffer Strength ⁽⁹⁾ (mA)	Power Supply ⁽¹⁰⁾
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
M21	PC5	Input	0	Function7	I	PU	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_RB0	2		I				
		SDC2_CMD	3		I/O				
		SPI0_CS	4		I/O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
N22	PC6	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ0	2		I/O				
		SDC2_D0	3		I/O				
		SPI0_HOLD	4		I/O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
N23	PC7	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ1	2		I/O				
		SDC2_D1	3		I/O				
		SPI0_WP	4		I/O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
R22	PC8	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ2	2		I/O				
		SDC2_D2	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
R23	PC9	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ3	2		I/O				
		SDC2_D3	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
T22	PC10	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ4	2		I/O				
		SDC2_D4	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
T21	PC11	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ5	2		I/O				
		SDC2_D5	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
U19	PC12	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				

Ball# ⁽¹⁾	Pin Name ⁽²⁾	Signal Name ⁽³⁾	Function ⁽⁴⁾	Ball Reset Rel. Function ⁽⁵⁾	Type ⁽⁶⁾	Ball Reset State ⁽⁷⁾	Pull Up/Down ⁽⁸⁾	Buffer Strength ⁽⁹⁾ (mA)	Power Supply ⁽¹⁰⁾
		NAND_DQ6	2		I/O				
		SDC2_D6	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
U21	PC13	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ7	2		I/O				
		SDC2_D7	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
R19	PC14	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQS	2		I/O				
		SDC2_RST	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
P19	PC15	Input	0	Function7	I	PU	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_CE1	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
P21	PC16	Input	0	Function7	I	PU	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_RB1	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
N19	VCC-PC	VCC-PC	NA	NA	P	NA	NA	NA	NA
GPIOD									
N3	PD0	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		LCD0_D2	2		O				
		TS0_CLK	3		I				
		CSI_PCLK	4		I				
		RGMII_RXD3/ RMII_NULL	5		I				
		Reserved	6		NA				
		IO disable	7		OFF				
M3	PD1	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		LCD0_D3	2		O				
		TS0_ERR	3		I				
		CSI_MCLK	4		O				
		RGMII_RXD2/ RMII_NULL	5		I				
		Reserved	6		NA				
		IO disable	7		OFF				
L6	PD2	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		LCD0_D4	2		O				
		TS0_SYNC	3		I				
		CSI_HSYNC	4		I				

Ball# ⁽¹⁾	Pin Name ⁽²⁾	Signal Name ⁽³⁾	Function ⁽⁴⁾	Ball Reset Rel. Function ⁽⁵⁾	Type ⁽⁶⁾	Ball Reset State ⁽⁷⁾	Pull Up/Down ⁽⁸⁾	Buffer Strength ⁽⁹⁾ (mA)	Power Supply ⁽¹⁰⁾
		RGMII_RXD1/ RMII_RXD1	5		I				
		Reserved	6		NA				
		IO disable	7		OFF				
M5	PD3	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		LCD0_D5	2		O				
		TS0_DVLD	3		I				
		CSI_VSYNC	4		I				
		RGMII_RXD0/ RMII_RXD0	5		I				
		Reserved	6		NA				
		IO disable	7		OFF				
M2	PD4	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		LCD0_D6	2		O				
		TS0_D0	3		I				
		CSI_D0	4		I				
		RGMII_RXCK/ RMII_NULL	5		I				
		Reserved	6		NA				
		IO disable	7		OFF				
M4	PD5	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		LCD0_D7	2		O				
		TS0_D1	3		I				
		CSI_D1	4		I				
		RGMII_RXCTL/ RMII_CRS_DV	5		I				
		Reserved	6		NA				
		IO disable	7		OFF				
N2	PD6	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		LCD0_D10	2		O				
		TS0_D2	3		I				
		CSI_D2	4		I				
		RGMII_NULL/ RMII_RXER	5		I				
		Reserved	6		NA				
		IO disable	7		OFF				
T1	PD7	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		LCD0_D11	2		O				
		TS0_D3	3		I				
		CSI_D3	4		I				
		RGMII_TXD3/ RMII_NULL	5		O				
		Reserved	6		NA				
		IO disable	7		OFF				
P5	PD8	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		LCD0_D12	2		O				
		TS0_D4	3		I				
		CSI_D4	4		I				
		RGMII_TXD2/ RMII_NULL	5		O				
		Reserved	6		NA				
		IO Disable	7		OFF				
P2	PD9	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		LCD0_D13	2		O				
		TS0_D5	3		I				

Ball# ⁽¹⁾	Pin Name ⁽²⁾	Signal Name ⁽³⁾	Function ⁽⁴⁾	Ball Reset Rel. Function ⁽⁵⁾	Type ⁽⁶⁾	Ball Reset State ⁽⁷⁾	Pull Up/Down ⁽⁸⁾	Buffer Strength ⁽⁹⁾ (mA)	Power Supply ⁽¹⁰⁾
		CSI_D5	4		I				
		RGMII_TXD1/ RMII_TXD1	5		O				
		Reserved	6		NA				
		IO Disable	7		OFF				
M6	PD10	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		LCD0_D14	2		O				
		TS0_D6	3		I				
		CSI_D6	4		I				
		RGMII_TXD0/ RMII_TXD0	5		O				
		Reserved	6		NA				
		IO Disable	7		OFF				
P1	PD11	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		LCD0_D15	2		O				
		TS0_D7	3		I				
		CSI_D7	4		I				
		RGMII_TXCK/ RMII_TXCK	5		I/O				
		Reserved	6		NA				
		IO Disable	7		OFF				
V2	PD12	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		LCD0_D18	2		O				
		TS1_CLK	3		I				
		CSI_SCK	4		O				
		RGMII_TXCTL/ RMII_TXEN	5		O				
		Reserved	6		NA				
		IO Disable	7		OFF				
P6	PD13	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		LCD0_D19	2		O				
		TS1_ERR	3		I				
		CSI_SDA	4		I/O				
		RGMII_CLKIN/ RMII_NULL	5		I				
		Reserved	6		NA				
		IO Disable	7		OFF				
U4	PD14	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		LCD0_D20	2		O				
		TS1_SYNC	3		I				
		DMIC_CLK	4		O				
		CSI_D8	5		I				
		Reserved	6		NA				
		IO Disable	7		OFF				
R3	PD15	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		LCD0_D21	2		O				
		TS1_DVLD	3		I				
		DMIC_DATA0	4		I				
		CSI_D9	5		I				
		Reserved	6		NA				
		IO Disable	7		OFF				
R2	PD16	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		LCD0_D22	2		O				
		TS1_D0	3		I				
		DMIC_DATA1	4		I				
		Reserved	5		NA				

Ball# ⁽¹⁾	Pin Name ⁽²⁾	Signal Name ⁽³⁾	Function ⁽⁴⁾	Ball Reset Rel. Function ⁽⁵⁾	Type ⁽⁶⁾	Ball Reset State ⁽⁷⁾	Pull Up/Down ⁽⁸⁾	Buffer Strength ⁽⁹⁾ (mA)	Power Supply ⁽¹⁰⁾
		Reserved	6		NA				
		IO Disable	7		OFF				
T2	PD17	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		LCD0_D23	2		O				
		TS2_CLK	3		I				
		DMIC_DATA2	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
P4	PD18	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		LCD0_CLK	2		O				
		TS2_ERR	3		I				
		DMIC_DATA3	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
P3	PD19	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		LCD0_DE	2		O				
		TS2_SYNC	3		I				
		UART2_TX	4		O				
		MDC	5		O				
		Reserved	6		NA				
		IO Disable	7		OFF				
V3	PD20	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		LCD0_HSYNC	2		O				
		TS2_DVLD	3		I				
		UART2_RX	4		I				
		MDIO	5		I/O				
		Reserved	6		NA				
		IO Disable	7		OFF				
T3	PD21	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		LCD0_VSYNC	2		O				
		TS2_D0	3		I				
		UART2_RTS	4		O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
U2	PD22	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		PWM0	2		O				
		TS3_CLK	3		I				
		UART2_CTS	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
U5	PD23	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		TWI2_SCK	2		I/O				
		TS3_ERR	3		I				
		UART3_TX	4		O				
		JTAG_MS	5		I				
		Reserved	6		NA				
		IO Disable	7		OFF				
V1	PD24	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		TWI2_SDA	2		I/O				
		TS3_SYNC	3		I				

Ball# ⁽¹⁾	Pin Name ⁽²⁾	Signal Name ⁽³⁾	Function ⁽⁴⁾	Ball Reset Rel. Function ⁽⁵⁾	Type ⁽⁶⁾	Ball Reset State ⁽⁷⁾	Pull Up/Down ⁽⁸⁾	Buffer Strength ⁽⁹⁾ (mA)	Power Supply ⁽¹⁰⁾
		UART3_RX	4		I				
		JTAG_CK	5		I				
		Reserved	6		NA				
		IO Disable	7		OFF				
U3	PD25	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		TWI0_SCK	2		I/O				
		TS3_DVLD	3		I				
		UART3_RTS	4		O				
		JTAG_DO	5		O				
		Reserved	6		NA				
		IO Disable	7		OFF				
R5	PD26	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		TWI0_SDA	2		I/O				
		TS3_D0	3		I				
		UART3_CTS	4		I				
		JTAG_DI	5		I				
		Reserved	6		NA				
		IO disable	7		OFF				
R6	VCC-PD	VCC-PD	NA	NA	P	NA	NA	NA	NA
GPIOF									
E2	PF0	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SDC0_D1	2		I/O				
		JTAG_MS1	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT0	6		I				
		IO Disable	7		OFF				
F3	PF1	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SDC0_D0	2		I/O				
		JTAG_DI1	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT1	6		I				
		IO Disable	7		OFF				
F2	PF2	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SDC0_CLK	2		O				
		UART0_TX	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT2	6		I				
		IO Disable	7		OFF				
G3	PF3	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SDC0_CMD	2		I/O				
		JTAG_DO1	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT3	6		I				
		IO Disable	7		OFF				
F1	PF4	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SDC0_D3	2		I/O				
		UART0_RX	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT4	6		I				
		IO Disable	7		OFF				

Ball# ⁽¹⁾	Pin Name ⁽²⁾	Signal Name ⁽³⁾	Function ⁽⁴⁾	Ball Reset Rel. Function ⁽⁵⁾	Type ⁽⁶⁾	Ball Reset State ⁽⁷⁾	Pull Up/Down ⁽⁸⁾	Buffer Strength ⁽⁹⁾ (mA)	Power Supply ⁽¹⁰⁾
G2	PF5	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SDC0_D2	2		I/O				
		JTAG_CK1	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT5	6		I				
		IO Disable	7		OFF				
C8	PF6	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT6	6		I				
		IO Disable	7		OFF				
GPIOG									
J2	PG0	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_CLK	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT0	6		I				
		IO Disable	7		OFF				
J3	PG1	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_CMD	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT1	6		I				
		IO Disable	7		OFF				
J5	PG2	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_D0	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT2	6		I				
		IO Disable	7		OFF				
H2	PG3	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_D1	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT3	6		I				
		IO Disable	7		OFF				
L5	PG4	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_D2	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT4	6		I				
		IO Disable	7		OFF				
H5	PG5	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_D3	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				

Ball# ⁽¹⁾	Pin Name ⁽²⁾	Signal Name ⁽³⁾	Function ⁽⁴⁾	Ball Reset Rel. Function ⁽⁵⁾	Type ⁽⁶⁾	Ball Reset State ⁽⁷⁾	Pull Up/Down ⁽⁸⁾	Buffer Strength ⁽⁹⁾ (mA)	Power Supply ⁽¹⁰⁾
		Reserved	5		NA				
		PG_EINT5	6		I				
		IO Disable	7		OFF				
H4	PG6	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		UART1_TX	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT6	6		I				
		IO Disable	7		OFF				
J6	PG7	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		UART1_RX	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT7	6		I				
		IO Disable	7		OFF				
H3	PG8	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		UART1_RTS	2		O				
		Reserved	3		NA				
		SIM0_VPPEN	4		O				
		Reserved	5		NA				
		PG_EINT8	6		I				
		IO Disable	7		OFF				
K1	PG9	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		UART1_CTS	2		I				
		Reserved	3		NA				
		SIM0_VPPPP	4		O				
		Reserved	5		NA				
		PG_EINT9	6		I				
		IO Disable	7		OFF				
K3	PG10	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		PCM2_SYNC	2		I/O				
		H_PCM2_SYNC	3		I/O				
		SIM0_PWREN	4		O				
		Reserved	5		NA				
		PG_EINT10	6		I				
		IO Disable	7		OFF				
K2	PG11	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		PCM1_CLK	2		I/O				
		H_PCM2_CLK	3		I/O				
		SIM0_CLK	4		O				
		Reserved	5		NA				
		PG_EINT11	6		I				
		IO Disable	7		OFF				
L3	PG12	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		PCM2_DOUT	2		O				
		H_PCM2_DOUT	3		O				
		SIM0_DATA	4		I/O				
		Reserved	5		NA				
		PG_EINT12	6		I				
		IO Disable	7		OFF				
L4	PG13	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		PCM2_DIN	2		I				

Ball# ⁽¹⁾	Pin Name ⁽²⁾	Signal Name ⁽³⁾	Function ⁽⁴⁾	Ball Reset Rel. Function ⁽⁵⁾	Type ⁽⁶⁾	Ball Reset State ⁽⁷⁾	Pull Up/Down ⁽⁸⁾	Buffer Strength ⁽⁹⁾ (mA)	Power Supply ⁽¹⁰⁾
		H_PCM2_DIN	3		I				
		SIM0_RST	4		O				
		Reserved	5		NA				
		PG_EINT13	6		I				
		IO Disable	7		OFF				
L2	PG14	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		PCM2_MCLK	2		O				
		H_PCM2_MCLK	3		O				
		SIM0_DET	4		I				
		Reserved	5		NA				
		PG_EINT14	6		I				
		IO Disable	7		OFF				
H6	VCC-PG	VCC-PG	NA	NA	P	NA	NA	NA	NA
GPIO H									
C9	PH0	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART0_TX	2		O				
		PCM0_SYNC	3		I/O				
		H_PCM0_SYNC	4		I/O				
		SIM1_VPPEN	5		O				
		PH_EINT0	6		I				
		IO Disable	7		OFF				
D12	PH1	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART0_RX	2		I				
		PCM0_CLK	3		I/O				
		H_PCM0_CLK	4		I/O				
		SIM1_VPPPP	5		O				
		PH_EINT1	6		I				
		IO Disable	7		OFF				
E11	PH2	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CIR_TX	2		O				
		PCM0_DOUT	3		O				
		H_PCM0_DOUT	4		O				
		SIM1_PWREN	5		O				
		PH_EINT2	6		I				
		IO Disable	7		OFF				
D11	PH3	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SPI1_CS	2		I/O				
		PCM0_DIN	3		I				
		H_PCM0_DIN	4		I				
		SIM1_CLK	5		O				
		PH_EINT3	6		I				
		IO Disable	7		OFF				
E12	PH4	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SPI1_CLK	2		I/O				
		PCM0_MCLK	3		O				
		H_PCM0_MCLK	4		O				
		SIM1_DATA	5		I/O				
		PH_EINT4	6		I				
		IO Disable	7		OFF				
F9	PH5	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SPI1_MOSI	2		I/O				
		OWA_MCLK	3		O				
		TWI1_SCK	4		I/O				
		SIM1_RST	5		O				
		PH_EINT5	6		I				

Ball# ⁽¹⁾	Pin Name ⁽²⁾	Signal Name ⁽³⁾	Function ⁽⁴⁾	Ball Reset Rel. Function ⁽⁵⁾	Type ⁽⁶⁾	Ball Reset State ⁽⁷⁾	Pull Up/Down ⁽⁸⁾	Buffer Strength ⁽⁹⁾ (mA)	Power Supply ⁽¹⁰⁾
		IO Disable	7		OFF				
D9	PH6	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SPI1_MISO	2		I/O				
		OWA_IN	3		I				
		TWI1_SDA	4		I/O				
		SIM1_DET	5		I				
		PH_EINT6	6		I				
		IO Disable	7		OFF				
F8	PH7	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		Reserved	2		NA				
		OWA_OUT	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PH_EINT7	6		I				
		IO Disable	7		OFF				
E10	PH8	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		HSCL	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PH_EINT8	6		I				
		IO Disable	7		OFF				
F7	PH9	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		HSDA	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PH_EINT9	6		I				
		IO Disable	7		OFF				
E9	PH10	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		HCEC	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PH_EINT10	6		I				
		IO Disable	7		OFF				
GPIOI									
K20	PL0	Input	0	Function7	I	PU	PU/PD	20	VCC-PL
		Output	1		O				
		Reserved	2		NA				
		S_TWI_SCK	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT0	6		I				
		IO Disable	7		OFF				
K23	PL1	Input	0	Function7	I	PU	PU/PD	20	VCC-PL
		Output	1		O				
		Reserved	2		NA				
		S_TWI_SDA	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT1	6		I				
		IO Disable	7		OFF				
K22	PL2	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_UART_TX	2		O				
		Reserved	3		NA				

Ball# ⁽¹⁾	Pin Name ⁽²⁾	Signal Name ⁽³⁾	Function ⁽⁴⁾	Ball Reset Rel. Function ⁽⁵⁾	Type ⁽⁶⁾	Ball Reset State ⁽⁷⁾	Pull Up/Down ⁽⁸⁾	Buffer Strength ⁽⁹⁾ (mA)	Power Supply ⁽¹⁰⁾
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT2	6		I				
		IO Disable	7		OFF				
J20	PL3	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_UART_RX	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT3	6		I				
		IO Disable	7		OFF				
K21	PL4	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_JTAG_MS	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT4	6		I				
		IO Disable	7		OFF				
J22	PL5	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_JTAG_CK	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT5	6		I				
		IO Disable	7		OFF				
H20	PL6	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_JTAG_DO	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT6	6		I				
		IO Disable	7		OFF				
J21	PL7	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_JTAG_DI	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT7	6		I				
		IO Disable	7		OFF				
H22	PL8	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_PWM0	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT8	6		I				
		IO Disable	7		OFF				
J19	PL9	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_CIR_RX	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT9	6		I				
		IO Disable	7		OFF				
H21	PL10	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				

Ball# ⁽¹⁾	Pin Name ⁽²⁾	Signal Name ⁽³⁾	Function ⁽⁴⁾	Ball Reset Rel. Function ⁽⁵⁾	Type ⁽⁶⁾	Ball Reset State ⁽⁷⁾	Pull Up/Down ⁽⁸⁾	Buffer Strength ⁽⁹⁾ (mA)	Power Supply ⁽¹⁰⁾
		S_OWC	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT10	6		I				
		IO Disable	7		OFF				
H18	VCC-PL	VCC-PL	NA	NA	P	NA	NA	NA	NA
GPIOM									
L20	PM0	Input	0	Funtion7	I	Z	PU/PD	20	VCC-PM
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PM_EINT0	6		I				
		IO Disable	7		OFF				
L21	PM1	Input	0	Function7	I	Z	PU/PD	20	VCC-PM
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PM_EINT1	6		I				
		IO Disable	7		OFF				
L22	PM2	Input	0	Function7	I	Z	PU/PD	20	VCC-PM
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PM_EINT2	6		I				
		IO Disable	7		OFF				
M22	PM3	Input	0	Function7	I	Z	PU/PD	20	VCC-PM
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PM_EINT3	6		I				
		IO Disable	7		OFF				
L19	PM4	Input	0	Function7	I	Z	PU/PD	20	VCC-PM
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PM_EINT4	6		I				
		IO Disable	7		OFF				
M19	VCC_PM	VCC-PM	NA	NA	P	NA	NA	NA	NA
System									
H19	TEST	TEST	NA	NA	I	PD	PU/PD	NA	VCC-RTC
G21	NMI	NMI	NA	NA	I/O	Z	PU/PD	NA	VCC-RTC
G22	RESET	RESET	NA	NA	I/O	Z	PU/PD	NA	VCC-RTC
F11	JTAG-SEL0	JTAG-SEL0	NA	NA	I	PU	PU/PD	NA	VCC-IO
G10	JTAG-SEL1	JTAG-SEL1	NA	NA	I	PU	PU/PD	NA	VCC-IO
E21	CLOCK-SELECT	CLOCK-SELECT	NA	NA	I/O	Z	PU/PD	NA	VCC-RTC
H17	BOOT-SELECT	BOOT-SELECT	NA	NA	I	PU	PU/PD	NA	VCC18-BIAS
G17	UBOOT	UBOOT	NA	NA	I	PU	PU/PD	NA	VCC18-BIAS
BIAS									
D21	BIAS-REXT	BIAS-REXT	NA	NA	AO	NA	NA	NA	VCC18-BIAS
D19	BIAS-VRAL	BIAS-VRAL	NA	NA	AO	NA	NA	NA	VCC18-BIAS
D21	BIAS-ITEST	BIAS-ITEST	NA	NA	AO	NA	NA	NA	VCC18-BIAS

Ball# ⁽¹⁾	Pin Name ⁽²⁾	Signal Name ⁽³⁾	Function ⁽⁴⁾	Ball Reset Rel. Function ⁽⁵⁾	Type ⁽⁶⁾	Ball Reset State ⁽⁷⁾	Pull Up/Down ⁽⁸⁾	Buffer Strength ⁽⁹⁾ (mA)	Power Supply ⁽¹⁰⁾
E19	VCC18-BIAS	VCC18-BIAS	NA	NA	P	NA	NA	NA	NA
TV-OUT									
A3	TVOUT	TVOUT	NA	NA	AO	NA	NA	NA	VCC-TV
C3	VCC-TV	VCC-TV	NA	NA	P	NA	NA	NA	NA
EPHY									
B7	EPHY-LNK-LED	EPHY-LINK-LED	NA	NA	O	NA	NA	NA	VCC-EPHY
C5	EPHY-SPD-LED	EPHY-SPD-LED	NA	NA	O	NA	NA	NA	VCC-EPHY
B4	EPHY-RTX	EPHY-RTX	NA	NA	A I/O	NA	NA	NA	VCC-EPHY
B6	EPHY-RXN	EPHY-RXN	NA	NA	A I/O	NA	NA	NA	VCC-EPHY
A6	EPHY-RXP	EPHY-RXP	NA	NA	A I/O	NA	NA	NA	VCC-EPHY
B5	EPHY-TXN	EPHY-TXN	NA	NA	A I/O	NA	NA	NA	VCC-EPHY
A5	EPHY-TXP	EPHY-TXP	NA	NA	A I/O	NA	NA	NA	VCC-EPHY
B3	VCC-EPHY	VCC-EPHY	NA	NA	P	NA	NA	NA	NA
Audio Codec									
D2	LINEOUTL	LINEOUTL	NA	NA	AO	NA	NA	NA	AC-AVCC
D1	LINEOUTR	LINEOUTR	NA	NA	AO	NA	NA	NA	AC-AVCC
F5	MBIAS	MBIAS	NA	NA	AO	NA	NA	NA	AC-AVCC
C4	VRA1	VRA1	NA	NA	AO	NA	NA	NA	AC-AVCC
D4	VRA2	VRA2	NA	NA	AO	NA	NA	NA	AC-AVCC
C2	MIC1N	MIC1N	NA	NA	AI	NA	NA	NA	AC-AVCC
C1	MIC1P	MIC1P	NA	NA	AI	NA	NA	NA	AC-AVCC
B2	MIC2N	MIC2N	NA	NA	AI	NA	NA	NA	AC-AVCC
B1	MIC2P	MIC2P	NA	NA	AI	NA	NA	NA	AC-AVCC
D3	AC-AVCC	AC-AVCC	NA	NA	P	NA	NA	NA	NA
E4	AC-LDOIN	AC-LDOIN	NA	NA	P	NA	NA	NA	NA
A1,E1,E3,E5	AGND	AGND	NA	NA	G	NA	NA	NA	NA
System									
E6	AC-SYS-VDD-IN	AC-SYS-VDD-IN	NA	NA	AI	NA	NA	NA	AC-AVCC
D5	AC-SYS-VDD-OUT	AC-SYS-VDD-OUT	NA	NA	AO	NA	NA	NA	AC-AVCC
HDMI									
C20	HHPD	HHPD	NA	NA	I/O	NA	NA	NA	VCC18-HDMI
A19	HTX0P	HTX0P	NA	NA	AO	NA	NA	NA	VCC18-HDMI
B19	HTX0N	HTX0N	NA	NA	AO	NA	NA	NA	VCC18-HDMI
A18	HTX1P	HTX1P	NA	NA	AO	NA	NA	NA	VCC18-HDMI
B18	HTX1N	HTX1N	NA	NA	AO	NA	NA	NA	VCC18-HDMI
A17	HTX2P	HTX2P	NA	NA	AO	NA	NA	NA	VCC18-HDMI
B17	HTX2N	HTX2N	NA	NA	AO	NA	NA	NA	VCC18-HDMI
A20	HTXCP	HTXCP	NA	NA	AO	NA	NA	NA	VCC18-HDMI
B20	HTXCN	HTXCN	NA	NA	AO	NA	NA	NA	VCC18-HDMI
C19	VCC18-HDMI	VCC18-HDMI	NA	NA	P	NA	NA	NA	NA
D18	VDD09-HDMI	VDD09-HDMI	NA	NA	P	NA	NA	NA	NA
USB									
A13	USB0-DM	USB0-DM	NA	NA	A I/O	NA	NA	NA	VCC-USB
B13	USB0-DP	USB0-DP	NA	NA	A I/O	NA	NA	NA	VCC-USB
B16	USB1-DM	USB1-DM	NA	NA	A I/O	NA	NA	NA	VCC-USB
C16	USB1-DP	USB1-DP	NA	NA	A I/O	NA	NA	NA	VCC-USB
B15	USB1-SSTXN	USB1-SSTXN	NA	NA	A I/O	NA	NA	NA	VCC-USB
C15	USB1-SSTXP	USB1-SSTXP	NA	NA	A I/O	NA	NA	NA	VCC-USB
A14	USB1-SSRXN	USB1-SSRXN	NA	NA	A I/O	NA	NA	NA	VCC-USB
B14	USB1-SSRXP	USB1-SSRXP	NA	NA	A I/O	NA	NA	NA	VCC-USB
A12	USB2-DM	USB2-DM	NA	NA	A I/O	NA	NA	NA	VCC-USB
B12	USB2-DP	USB2-DP	NA	NA	A I/O	NA	NA	NA	VCC-USB
E14	VCC-USB	VCC-USB	NA	NA	P	NA	NA	NA	NA
G16	VDD-USB	VDD-USB	NA	NA	P	NA	NA	NA	NA
PCIe									
A8	PCIe-REF-CLKP	PCIe-REF-CLKP	NA	NA	A I/O	NA	NA	NA	VCC-PCIe
B8	PCIe-REF-CLKM	PCIe-REF-CLKM	NA	NA	A I/O	NA	NA	NA	VCC-PCIe
A9	PCIe-TXP	PCIe-TXP	NA	NA	A I/O	NA	NA	NA	VCC-PCIe
B9	PCIe-TXM	PCIe-TXM	NA	NA	A I/O	NA	NA	NA	VCC-PCIe
A10	PCIe-RXP	PCIe-RXP	NA	NA	A I/O	NA	NA	NA	VCC-PCIe
B10	PCIe-RXM	PCIe-RXM	NA	NA	A I/O	NA	NA	NA	VCC-PCIe
H11	VCC-PCIe	VCC-PCIe	NA	NA	P	NA	NA	NA	NA



Ball# ⁽¹⁾	Pin Name ⁽²⁾	Signal Name ⁽³⁾	Function ⁽⁴⁾	Ball Reset Rel. Function ⁽⁵⁾	Type ⁽⁶⁾	Ball Reset State ⁽⁷⁾	Pull Up/Down ⁽⁸⁾	Buffer Strength ⁽⁹⁾ (mA)	Power Supply ⁽¹⁰⁾
G12	VDD09-PCIE	VDD09-PCIE	NA	NA	P	NA	NA	NA	NA
HSIC									
D15	HSIC-STR	HSIC-STR	NA	NA	A I/O	NA	NA	NA	HSIC-VCC
E17	HSIC-DAT	HSIC-DAT	NA	NA	A I/O	NA	NA	NA	HSIC-VCC
D16	HSIC-VCC	HSIC-VCC	NA	NA	P	NA	NA	NA	NA
Clock									
V22	X24MIN	X24MIN	NA	NA	AI	NA	NA	NA	VCC-PLL
V23	X24MOUT	X24MOUT	NA	NA	AO	NA	NA	NA	VCC-PLL
V21	PLL-TEST	PLL-TEST	NA	NA	AOD	NA	NA	NA	VCC-PLL
P18	VCC-PLL	VCC-PLL	NA	NA	P	NA	NA	NA	NA
DCXO									
B23	DXIN	DXIN	NA	NA	AI	NA	NA	NA	VCC-RTC
B22	DXOUT	DXOUT	NA	NA	AO	NA	NA	NA	VCC-RTC
E22	WREQIN	WREQIN	NA	NA	AI	NA	NA	NA	VCC-RTC
C23	REFCLK-OUT	REFCLK-OUT	NA	NA	AO	NA	NA	NA	VCC-RTC
D22	DXLDO-OUT	DXLDO-OUT	NA	NA	P	NA	NA	NA	NA
A22	DXVCCIO	DXVCCIO	NA	NA	P	NA	NA	NA	NA
RTC									
F23	X32KIN	X32KIN	NA	NA	AI	NA	NA	NA	VCC-RTC
F22	X32KOUT	X32KOUT	NA	NA	AO	NA	NA	NA	VCC-RTC
G20	X32KFOUT	X32KFOUT	NA	NA	AOD	NA	NA	NA	VCC-RTC
F20	VCC-RTC	VCC-RTC	NA	NA	P	NA	NA	NA	NA
F19	RTC-VIO	RTC-VIO	NA	NA	AO	NA	NA	NA	VCC-RTC
Other									
E8	TEST1	TEST1	NA	NA	I/O	NA	NA	NA	AC-LDOIN
C7	TEST2	TEST2	NA	NA	I/O	NA	NA	NA	AC-LDOIN
E7	TEST3	TEST3	NA	NA	I/O	NA	NA	NA	AC-LDOIN
Power									
R7	VDD-GPUFB	VDD-GPUFB	NA	NA	P	NA	NA	NA	NA
G8	VCC-IO	VCC-IO	NA	NA	P	NA	NA	NA	NA
L16,L17,M16,M17, N16,N17,P15,P16, P17	VDD-CPU	VDD-CPU	NA	NA	P	NA	NA	NA	NA
K18	VDD-CPUS	VDD-CPUS	NA	NA	P	NA	NA	NA	NA
H10,J10,J11,K10,K11, K12,L10,L11,L12,L13, L14	VDD-SYS	VDD-SYS	NA	NA	P	NA	NA	NA	NA
R16, T16	VDD-CPUFB	VDD-CPUFB	NA	NA	P	NA	NA	NA	NA
L8,M8,M9,N8,N9,P8, P9	VDD-GPU	VDD-GPU	NA	NA	P	NA	NA	NA	NA
EFUSE									
G11	VDD-EFUSE	VDD-EFUSE	NA	NA	P	NA	NA	NA	NA
Ground									
A16,A21,A23,C12, C13,C14,C18,C22, D23,E13,E15,E16, E18,F12,F13,F14,F15, F16,F17,G7,G9,G15, H1,H7,H8,H9,H10, H12,H15,H16,H23,J7, J8,J9,J10,J11,J12,J15, J16,J17,K7,K8,K9,K10, K11,K12,K13,K14, K15,K16,K17,L7,L9, L10,L11,L12,L13,L14, L15,L18,M1,M7,M10, M11,M12,M13,M14, M15,M18,M23,N7, N10,N11,N12,N13, N14,N15,N18,P7,P10, P11,P12,P13,P14, P20,R8,R9,R10,R11, R12,R13,R14,R15,	GND	GND	NA	NA	G	NA	NA	NA	NA

Ball# ⁽¹⁾	Pin Name ⁽²⁾	Signal Name ⁽³⁾	Function ⁽⁴⁾	Ball Reset Rel. Function ⁽⁵⁾	Type ⁽⁶⁾	Ball Reset State ⁽⁷⁾	Pull Up/Down ⁽⁸⁾	Buffer Strength ⁽⁹⁾ (mA)	Power Supply ⁽¹⁰⁾
R17,R18,T7,T8,T9, T10,T11,T12,T13,T14, T15,T16,T18,T19,U6, U7,U9,U10,U11,U12, U15,U17,U18,U22, U23,V5,V7,V13,V17, V19,V20,W1,W3, W10,W21,W23,Y5, Y13,Y19,AA8,AA16, AA21,AB3,AB13, AB21,AC1,AC5,AC11, AC19, AC23									

4.2. Signal Descriptions

H6 V200 contains many peripheral interfaces. Many of the interfaces can multiplex up to eight functions. Pin-multiplexing configuration can refer to Table 4-1. Table 4-2 shows the detailed function description of every signal based on the different interface.

(1).**Signal Name**: The name of every signal.

(2).**Description**: The detailed function description of every signal.

(3).**Type**: Denotes the signal direction:

I (Input),
O (Output),
I/O(Input/Output),
OD(Open-Drain),
A (Analog),
AI(Analog Input),
AO(Analog Output),
A I/O(Analog Input/Output),
P (Power),
G (Ground)

Table 4-2. Signal Descriptions

Signal Name ⁽¹⁾	Description ⁽²⁾	Type ⁽³⁾
DRAM		
SDQ[31:0]	DRAM Bidirectional Data Line to the Memory Device	I/O
SDQS[3:0]P	DRAM Active-High Bidirectional Data Strokes to the Memory Device	I/O
SDQS[3:0]N	DRAM Active-Low Bidirectional Data Strokes to the Memory Device	I/O
SDQM[3:0]	DRAM Data Mask Signal to the Memory Device	I/O
SCKP	DRAM Active-High Clock Signal to the Memory Device	O
SCKN	DRAM Active-Low Clock Signal to the Memory Device	O
SCKE[1:0]	DRAM Clock Enable Signal to the Memory Device for Two Chip Select	O
SA[13:0]	DRAM Address Signal to the Memory Device	O
SWE/SA14	DRAM Write Enable Strobe to the Memory Device/Address Signal to the Memory Device	O
SCAS/SA15	DRAM Column Address Strobe to the Memory Device/Address Signal to the Memory Device	O
SRAS/SA16	DRAM Row Address strobe to the Memory Device/Address Signal to the Memory Device	O
SA17	DRAM Address Signal to the Memory Device	O
SACT	DRAM Activation Command Output	O
SPAR	DRAM Command and Address Parity Output	O
SALERT	DRAM CRC Error Flag to the Memory Device	I
SCS[1:0]	DRAM Chip Select Signal to the Memory Device	O
SBA[1:0]	DRAM Bank Address Signal to the Memory Device	O

Signal Name ⁽¹⁾	Description ⁽²⁾	Type ⁽³⁾
SBG[1:0]	DRAM Bank Group Address to the Memory Device	O
SODT[1:0]	DRAM On-Die Termination Output Signal for Two Chip Select	O
SRST	DRAM Reset Signal to the Memory Device	O
SZQ	DRAM External Reference Resistor for Impedance Calibration	AI
SVREF	DRAM Reference Input	P
VCC-DRAM	DRAM Power Supply	P
VDD18-DRAM	Power Supply for DRAM Controller	P
System		
UBOOT	UBOOT Mode Select	I
BOOT-SELECT	Boot Media Select	I
TEST	TEST Signal	I
NMI	Non-Maskable Interrupt	I/O
RESET	Reset Signal	I/O
JTAG-SEL0	JTAG Mode Select 0	I
JTAG-SEL1	JTAG Mode Select 1	I
CLOCK-SELECT	Clock Select Signal	I/O
PLL&Clock		
X32KFOUT	32KHz Clock Fanout	AOD
X32KIN	Clock Input Of 32KHz Crystal	AI
X32KOUT	Clock Output Of 32KHz Crystal	AO
VCC-RTC	RTC Power Supply	P
RTC-VIO	Internal LDO Output Bypass	AO
X24MIN	Clock Input Of 24MHz Crystal	AI
X24MOUT	Clock Output Of 24MHz Crystal	AO
PLL-TEST	PLL Test	AOD
VCC-PLL	PLL Power Supply	P
DCXO		
DXIN	Digital Compensated Crystal Oscillator Input	AI
DXOUT	Digital Compensated Crystal Oscillator Output	AO
WREQIN	Digital Compensated Crystal Oscillator Wakeup Signal, High Active	AI
REFCLK-OUT	Digital Compensated Crystal Oscillator Clock Fanout	AO
DXLDO-OUT	Internal Supply Regulator Output	P
DXVCCIO	Digital Compensated Crystal Oscillator Power Supply	P
HDMI		
HTX0P	HDMI Positive TMDS Differential Line Driver Data0 Output	AO
HTX0N	HDMI Negative TMDS Differential Line Driver Data0 Output	AO
HTX1P	HDMI Positive TMDS Differential Line Driver Data1 Output	AO
HTX1N	HDMI Negative TMDS Differential Line Driver Data1 Output	AO
HTX2P	HDMI Positive TMDS Differential Line Driver Data2 Output	AO
HTX2N	HDMI Negative TMDS Differential Line Driver Data2 Output	AO
HTXCP	HDMI Positive TMDS Differential Line Driver Clock Output	AO
HTXCN	HDMI Negative TMDS Differential Line Driver Clock Output	AO

Signal Name ⁽¹⁾	Description ⁽²⁾	Type ⁽³⁾
HHPD	HDMI Hot Plug Detection Signal	I/O
HCEC	HDMI Consumer Electronics Control	I/O
HSCL	HDMI Serial Clock	O
HSDA	HDMI Serial Data	I/O
VCC18-HDMI	HDMI 1.8V Power Supply	P
VDD09-HDMI	HDMI 0.9V Power Supply	P
PCIe		
PCIE-REF-CLKP	PCIe Differential Signal REFCLK Positive	A I/O
PCIE-REF-CLKM	PCIe Differential Signal REFCLK Negative	A I/O
PCIE-TXP	PCIe Differential Signal Transmit Positive	A I/O
PCIE-TXM	PCIe Differential Signal Transmit Negative	A I/O
PCIE-RXP	PCIe Differential Signal Receive Positive	A I/O
PCIE-RXM	PCIe Differential Signal Receive Negative	A I/O
VCC-PCIE	PCIe 3.3V Power Supply	P
VDD09-PCIE	PCIe 0.9V Power Supply	P
USB		
USB0-DM	USB2.0 OTG DM Signal	A I/O
USB0-DP	USB2.0 OTG DP Signal	A I/O
USB1-DM	USB3.0 HOST DM Signal	A I/O
USB1-DP	USB3.0 HOST DP Signal	A I/O
USB1-SSRXN	USB3.0 HOST SuperSpeed Receive Negative Signal	A I/O
USB1-SSRXP	USB3.0 HOST SuperSpeed Receive Positive Signal	A I/O
USB1-SSTXN	USB3.0 HOST SuperSpeed Transmit Negative Signal	A I/O
USB1-SSTXP	USB3.0 HOST SuperSpeed Transmit Positive Signal	A I/O
USB2-DM	USB2.0 HOST DM Signal	A I/O
USB2-DP	USB2.0 HOST DP Signal	A I/O
VCC-USB	USB 3.3V Power Supply	P
VDD-USB	USB 0.9V Power Supply	P
HSIC		
HSIC-STR	HSIC Strobe Singal	A I/O
HSIC-DAT	HSIC Data Signal	A I/O
HSIC-VCC	HSIC Power Supply	P
EPHY		
EPHY-RXP	Transceiver Positive Output/Input	A I/O
EPHY-RXN	Transceiver Negative Output/Input	A I/O
EPHY-TXP	Transceiver Positive Output/Input	A I/O
EPHY-TXN	Transceiver Negative Output/Input	A I/O
EPHY-RTX	EPHY External Resistance to Ground	AI
EPHY-LINK-LED	EPHY LINK Up/Down Indicator LED	O
EPHY-SPD-LED	EPHY 10M/100M Indicator LED	O
VCC-EPHY	Power Supply for EPHY	P
TVOUT		

Signal Name ⁽¹⁾	Description ⁽²⁾	Type ⁽³⁾
TV-OUT	TV Output	AO
VCC-TV	TV Out Power Supply	P
Audio Codec		
LINEOUTL	LINE-OUT Left Channel Output	AO
LINEOUTR	LINE-OUT Right Channel Output	AO
MBIAS	Master Analog Microphone Bias	AO
MIC1N	Microphone Negative Input 1	AI
MIC1P	Microphone Positive Input 1	AI
MIC2N	Microphone Negative Input 2	AI
MIC2P	Microphone Positive Input 2	AI
VRA1	Reference Voltage Output	AO
VRA2	Reference Voltage Output	AO
AC-AVCC	Analog Power	P
AGND	Analog GND	G
I2S/PCM		
PCM0_SYNC	PCM 0 Sync/I2S 0 Left and Right Channel Select Clock	I/O
PCM0_CLK	PCM 0 Sample Rate Clock/I2S 0 Bit Clock	I/O
PCM0_DOUT	I2S 0/PCM 0 Serial Data Output	O
PCM0_DIN	I2S 0/PCM 0 Serial Data Input	I
PCM0_MCLK	I2S 0/PCM 0 Master Clock	O
PCM2_SYNC	PCM 2 Sync/I2S 2 Left and Right Channel Select Clock	I/O
PCM2_CLK	PCM 2 Sample Rate Clock/I2S 2 Bit Clock	I/O
PCM2_DOUT	I2S 2/PCM 2 Serial Data Output	O
PCM2_DIN	I2S 2/PCM 2 Serial Data Input	I
PCM2_MCLK	I2S 2/PCM 2 Master Clock	O
Audio HUB		
H_PCM0_SYNC	PCM 0 Sync/I2S 0 Left and Right Channel Select Clock	I/O
H_PCM0_CLK	PCM 0 Sample Rate Clock/I2S 0 Bit Clock	I/O
H_PCM0_DOUT	I2S 0/PCM 0 Serial Data Output	O
H_PCM0_DIN	I2S 0/PCM 0 Serial Data Input	I
H_PCM0_MCLK	I2S 0/PCM 0 Master Clock	O
H_PCM2_SYNC	PCM 2 Sync/I2S 2 Left and Right Channel Select Clock	I/O
H_PCM2_CLK	PCM 2 Sample Rate Clock/I2S 2 Bit Clock	I/O
H_PCM2_DOUT	I2S 2/PCM 2 Serial Data Output	O
H_PCM2_DIN	I2S 2/PCM 2 Serial Data Input	I
H_PCM2_MCLK	I2S 2/PCM 2 Master Clock	O
OWA		
OWA_IN	One Wire Audio Input	I
OWA_OUT	One Wire Audio Output	O
OWA_MCLK	One Wire Audio Master Clock	O
DMIC		
DMIC_CLK	Digital Microphone Clock Output	O
DMIC_DATA[3:0]	Digital Microphone Data Input	I

Signal Name ⁽¹⁾	Description ⁽²⁾	Type ⁽³⁾
SD/MMC		
SDC0_CMD	Command Signal for SD/TF Card	I/O
SDC0_CLK	Clock for SD/TF Card	O
SDC0_D[3:0]	Data Input and Output for SD/TF Card	I/O
SDC1_CMD	Command Signal for SDIO Wi-Fi	I/O
SDC1_CLK	Clock for SDIO Wi-Fi	O
SDC1_D[3:0]	Data Input and Output for SDIO Wi-Fi	I/O
SDC2_CMD	Command Signal for MMC	I/O
SDC2_CLK	Clock for MMC	O
SDC2_D[7:0]	Data Input and Output for MMC	I/O
SDC2_RST	Reset Signal for MMC	O
SDC2_DS	Data Strobe for MMC	I
NAND FLASH		
NAND_DQ[7:0]	NAND Flash0 Data Bit [7:0]	I/O
NAND_DQS	NAND Flash Data Strobe	I/O
NAND_WE	NAND Flash Write Enable	O
NAND_RE	NAND Flash Read Enable	O
NAND_ALE	NAND Flash Address Latch Enable	O
NAND_CLE	NAND Command Latch Enable	O
NAND_CE[1:0]	NAND Flash Chip Select [1:0]	O
NAND_RB[1:0]	NAND Flash Ready/Busy Bit	I
Interrupt		
PF_EINT[6:0]	GPIO F Interrupt	I
PG_EINT[14:0]	GPIO G Interrupt	I
PH_EINT[10:0]	GPIO H Interrupt	I
S_PL_EINT[10:0]	GPIO L Interrupt for CPUS	I
S_PM_EINT[4:0]	GPIO M Interrupt for CPUS	I
PWM		
S_PWM0	Pulse Width Modulation Output for CPUS	O
PWM0	Pulse Width Modulation Output	O
IR		
CIR_TX	Consumer IR Data Transmit	O
S_CIR_RX	Consumer IR Data Receive for CPUS	I
CSI		
CSI_PCLK	CSI Pixel Clock	I
CSI_MCLK	CSI Master Clock	O
CSI_HSYNC	CSI Horizontal SYNC	I
CSI_VSYNC	CSI Vertical SYNC	I
CSI_D[9:0]	CSI Data bit [9:0]	I
CSI_SCK	CSI Command Serial Clock Signal	O
CSI_SDA	CSI Command Serial Data Signal	I/O
LCD		

Signal Name ⁽¹⁾	Description ⁽²⁾	Type ⁽³⁾
LCD0_D[7:2]	LCD Data Bit for RGB/YUV Output	O
LCD0_D[15:10]		
LCD0_D[23:18]		
LCD0_CLK	LCD Clock Signal	O
LCD0_DE	LCD Data Enable	O
LCD0_HSYNC	LCD Horizontal Sync	O
LCD0_VSYNC	LCD Vertical Sync	O
EMAC		
RGMII_RXD3/RMII_NULL	RGMII Receive Data	I
RGMII_RXD2/RMII_NULL	RGMII Receive Data	I
RGMII_RXD1/RMII_RXD1	RGMII/RMII Receive Data	I
RGMII_RXD0/RMII_RXD0	RGMII/RMII Receive Data	I
RGMII_RXCK/RMII_NULL	RGMII Receive Clock	I
RGMII_RXCTL/RMII_CRS_DV	RGMII Receive Control /RMII Carrier Sense Receive Data Valid	I
RGMII_NULL/RMII_RXER	RMII Receive Error	I
RGMII_TXD3/RMII_NULL	RGMII Transmit Data	O
RGMII_TXD2/RMII_NULL	RGMII Transmit Data	O
RGMII_TXD1/RMII_TXD1	RGMII/RMII Transmit Data	O
RGMII_TXD0/RMII_TXD0	RGMII/RMII Transmit Data	O
RGMII_TXCK/RMII_TXCK	RGMII/RMII Transmit Clock: Output Pin for RGMII, Input Pin for RMII	I/O
RGMII_TXCTL/RMII_TXEN	RGMII Transmit Control/RMII Transmit Enable	O
RGMII_CLKIN/RMII_NULL	RGMII Transmit Clock from External	I
MDC	RGMII/RMII Management Data Clock	O
MDIO	RGMII/RMII Management Data Input/Output	I/O
Transport Stream Controller		
TS0_CLK	Transport Stream0 Clock	I
TS0_ERR	Transport Stream0 Error Indicate	I
TS0_SYNC	Transport Stream0 Sync	I
TS0_DVLD	Transport Stream0 Valid Signal	I
TS0_D[7:0]	Transport Stream0 Data	I
TS1_CLK	Transport Stream1 Clock	I
TS1_ERR	Transport Stream1 Error Indicate	I
TS1_SYNC	Transport Stream1 Sync	I
TS1_DVLD	Transport Stream1 Valid Signal	I
TS1_D0	Transport Stream1 Data	I
TS2_CLK	Transport Stream2 Clock	I
TS2_ERR	Transport Stream2 Error Indicate	I
TS2_SYNC	Transport Stream2 Sync	I
TS2_DVLD	Transport Stream2 Valid Signal	I
TS2_D0	Transport Stream2 Data	I
TS3_CLK	Transport Stream3 Clock	I
TS3_ERR	Transport Stream3 Error Indicate	I

Signal Name ⁽¹⁾	Description ⁽²⁾	Type ⁽³⁾
TS3_SYNC	Transport Stream3 Sync	I
TS3_DVLD	Transport Stream3 Valid Signal	I
TS3_D0	Transport Stream3 Data	I
SPI		
SPI0_CS	SPI0 Chip Select Signal, Low Active	I/O
SPI0_CLK	SPI0 Clock Signal	I/O
SPI0_MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0_MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0_HOLD	SPI0 Hold Signal	I/O
SPI0_WP	SPI0 Write Protect	I/O
SPI1_CS	SPI1 Chip Select signal, Low Active	I/O
SPI1_CLK	SPI1 Clock Signal	I/O
SPI1_MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1_MISO	SPI1 Master Data In, Slave Data Out	I/O
UART		
UART0_TX	UART0 Data Transmit	O
UART0_RX	UART0 Data Receive	I
UART1_TX	UART1 Data Transmit	O
UART1_RX	UART1 Data Receive	I
UART1_CTS	UART1 Data Clear To Send	I
UART1_RTS	UART1 Data Request To Send	O
UART2_TX	UART2 Data Transmit	O
UART2_RX	UART2 Data Receive	I
UART2_CTS	UART2 Data Clear To Send	I
UART2_RTS	UART2 Data Request To Send	O
UART3_TX	UART3 Data Transmit	O
UART3_RX	UART3 Data Receive	I
UART3_CTS	UART3 Data Clear To Send	I
UART3_RTS	UART3 Data Request To Send	O
S_UART_TX	UART Data Transmit for CPUS	O
S_UART_RX	UART Data Receive for CPUS	I
TWI (x=[2:0])		
TWix_SCK	TWix Serial Clock Signal	I/O
TWix_SDA	TWix Serial Data Signal	I/O
S_TWI_SCK	TWI Serial Clock Signal for CPUS	I/O
S_TWI_SDA	TWI Serial Data Signal for CPUS	I/O
Smart Card Reader(x=[1:0])		
SIMx_PWREN	Smart Card Power Enable	O
SIMx_CLK	Smart Card Clock	O
SIMx_DATA	Smart Card Data	I/O
SIMx_RST	Smart Card Reset	O
SIMx_DET	Smart Card Detect	I

Signal Name ⁽¹⁾	Description ⁽²⁾	Type ⁽³⁾
SIMx_VPPEN	Smart Card Program Voltage Enable	O
SIMx_VPPPP	Smart Card Vpp Pause and Program Control	O
One Wire		
S_OWC	One Wire Data Input/Output for CPUS	I/O
JTAG		
JTAG_MS	JTAG Mode Select Input	I
JTAG_CK	JTAG Clock Input	I
JTAG_DO	JTAG Data Output	O
JTAG_DI	JTAG Data Input	I
JTAG_MS1	JTAG Mode Select Input	I
JTAG_CK1	JTAG Clock Input	I
JTAG_DO1	JTAG Data Output	O
JTAG_DI1	JTAG Data Input	I
S_JTAG_MS	JTAG Mode Select Input for CPUS	I
S_JTAG_CK	JTAG Clock Input for CPUS	I
S_JTAG_DO	JTAG Data Output for CPUS	O
S_JTAG_DI	JTAG Data Input for CPUS	I

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 5-1 specifies the absolute maximum ratings over the operating junction temperature range of commercial and extended temperature devices.



CAUTION

Stresses beyond those listed under Table 5-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Section 5.2, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 5-1. Absolute Maximum Ratings

Symbol	Parameter	MIN	Max	Unit
I _{I/O}	In/Out Current for Input and Output	-40	40	mA
T _{STG}	Storage Temperature	-40	125	°C
AC-LDOIN	Power Supply for Analog Part	-0.3	3.6	V
VCC18-BIAS	Power Supply for Analog Part	-0.3	1.98	V
VCC-EPHY	Power Supply for EPHY	-0.3	3.6	V
VCC-TV	Power Supply for TV	-0.3	3.4	V
VCC18-HDMI	1.8V Power Supply for HDMI	-0.3	2.16	V
VDD09-HDMI	0.9V Power Supply for HDMI	-0.3	1.08	V
DXVCCIO	Power Supply for DCXO-IO	-0.3	1.98	V
VCC-IO	Power Supply for 3.3V Digital Part	-0.3	3.63	V
VCC-PC	Power Supply for Port C	-0.3	3.63	V
VCC-PD	Power Supply for Port D	-0.3	3.63	V
VCC-PG	Power Supply for Port G	-0.3	3.63	V
VCC-PL	Power Supply for Port L	-0.3	3.63	V
VCC-PM	Power Supply for Port M	-0.3	3.63	V
VCC-PLL	Power Supply for System PLL	-0.3	2.16	V
VCC-RTC	Power Supply for RTC	-0.3	2.16	V
VCC-USB	3.3V Power Supply for USB	-0.3	3.63	V
VDD-USB	0.9V Power Supply for USB	-0.3	0.99	V
HSIC-VCC	Power Supply for HSIC	-0.3	1.32	V
VCC-DRAM	Power Supply for DRAM	-0.3	1.98	V
VDD18-DRAM	Power Supply for DRAM	-0.3	1.98	V

VDD-CPUS	Power Supply for CPUS		-0.3	1.3	V
VDD-CPU	Power Supply for CPU		-0.3	1.3	V
VDD-GPU	Power Supply for GPU		-0.3	1.3	V
VCC-PCIE	1.8V Power Supply for PCIE		-0.3	2.16	V
	3.3V Power Supply for PCIE		-0.3	3.63	V
VDD09-PCIE	0.9V Power Supply for PCIE		-0.3	0.99	V
VDD-EFUSE	Power Supply for EFUSE		-0.3	2.16	V
VDD-SYS	Power Supply for System		-0.3	1.05	V
V _{ESD}	Electrostatic Discharge	Human Body Model(HBM) ⁽¹⁾	TBD	TBD	V
		Charged Device Model(CDM) ⁽²⁾	TBD	TBD	V
I _{Latch-up}	Latch-up I-test performance current-pulse injection on each IO pin ⁽³⁾		TBD		
	Latch-up over-voltage performance voltage injection on each IO pin ⁽⁴⁾		TBD		

1) Test method: JEDEC JS-001-2014(Class-3A). JEDEC publication JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

2) Test method: JS-002-2014(Class-C1). JEDEC publication JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

3) Current test performance: Pins stressed per JEDEC JESD78E(Class I, Level A) and passed with I/O pin injection current as defined in JEDEC.

4) Over voltage performance: Supplies stressed per JEDEC JESD78D(Class I, Level A) and passed voltage injection as defined in JEDEC.

5.2. Recommended Operating Conditions

All H6 V200 modules are used under the operating conditions contained in Table 5-2.



NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 5-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-20	-	+70	°C
Tj	Junction Temperature Range	-20	-	125	°C
AC-LDOIN	Power Supply for Analog Part	3.0	3.3	3.6	V
VCC18-BIAS	Power Supply for Analog Part	1.7	1.8	1.9	V
VCC-EPHY	3.3V Power Supply for EPHY	3.0	3.3	3.6	V
VCC-TV	Power Supply for TV	3.2	3.3	3.4	V
VCC18-HDMI	1.8V Power Supply for HDMI	1.62	1.8	1.98	V
VDD09-HDMI	0.9V Power Supply for HDMI	0.81	0.9	0.99	V
DXVCCIO	Power Supply for DCXO-IO	1.62	1.8	1.98	V
VCC-IO	Power Supply for 3.3V Digital Part	3.0	3.3	3.6	V

VCC-PC	Power Supply for Port C	1.7 3.0	1.8 3.3	1.98 3.6	V
VCC-PD	Power Supply for Port D	2.25 3.0	2.5 3.3	2.75 3.6	V
VCC-PG	Power Supply for Port G	1.7 3.0	1.8 3.3	1.98 3.6	V
VCC-PL	Power Supply for Port L	1.7 3.0	1.8 3.3	1.98 3.6	V
VCC-PM	Power Supply for Port M	1.7 3.0	1.8 3.3	1.98 3.6	V
VCC-PLL	Power Supply for System PLL	1.62	1.8	1.98	V
VCC-RTC	Power Supply for RTC	1.62	1.8	1.98	V
VCC-USB	3.3V Power Supply for USB	3.069	3.3	3.63	V
VDD-USB	0.9V Power Supply for USB	0.81	0.9	0.99	V
HSIC-VCC	Power Supply for HSIC	1.14	1.2	1.26	V
VCC-PCIE	1.8V/3.3V Power Supply for PCIE	1.67	1.8	1.98	V
		3.069	3.3	3.63	V
VDD09-PCIE	0.9V Power Supply for PCIE	0.837	0.9	0.99	V
VCC-DRAM	Power Supply for DDR4 IO Domain	1.14	1.2	1.26	V
	Power Supply for DDR3 IO Domain	1.425	1.5	1.575	V
	Power Supply for DDR3L IO Domain	1.425	1.5	1.575	V
	Power Supply for LPDDR2 IO Domain	1.14	1.2	1.3	V
	Power Supply for LPDDR3 IO Domain	1.14	1.2	1.3	V
VDD18-DRAM	Power Supply for DRAM Controller	1.71	1.8	1.89	V
VDD-CPUS	Power Supply for CPUS	0.873	0.9	0.927	V
VDD-CPU	Power Supply for CPU	0.81	-	1.08	V
VDD-GPU	Power Supply for GPU	0.81	-	1.08	V
VDD-EFUSE	Power Supply for EFUSE Program mode	1.8	1.9	1.98	V
VDD-SYS	Power Supply for System	0.92	0.96	1.0	V

5.3. DC Electrical Characteristics

Table 5-3 summarizes the DC electrical characteristics of H6 V200.

Table 5-3. DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V _{IH}	High-Level Input Voltage	0.7 * VCC-IO	-	VCC-IO + 0.3	V
V _{IL}	Low-Level Input Voltage	-0.3	-	0.3 * VCC-IO	V
R _{PU}	Input Pull-up Resistance	50	100	150	KΩ
R _{PD}	Input Pull-down Resistance	50	100	150	KΩ
I _{IH}	High-Level Input Current	-	-	10	uA
I _{IL}	Low-Level Input Current	-	-	10	uA

V _{OH}	High-Level Output Voltage	VCC-IO - 0.2	-	VCC-IO	V
V _{OL}	Low-Level Output Voltage	0	-	0.2	V
I _{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C _{IN}	Input Capacitance	-	-	5	pF
C _{OUT}	Output Capacitance	-	-	5	pF

5.4. Oscillator Electrical Characteristics

H6 V200 contains two external input clocks:X24MIN and X32KIN, two output clocks:X24MOUT and X32KOUT. The 24MHz frequency is used to generate the main source clock for PLL and the main digital blocks, the clock is provided through X24MIN.Table 5-4 lists the 24MHz crystal specifications.

Table 5-4. 24MHz Crystal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
1/(t _{CPMAIN})	Crystal Oscillator Frequency Range	-	24.000	-	MHz
t _{ST}	Startup Time	-	-	2	ms
	Frequency Tolerance at 25 °C	-50	-	+50	ppm
	Oscillation Mode	Fundamental			-
	Maximum Change Over Temperature Range	-50	-	+50	ppm
DL	Drive Level	-	-	300	uW
C _L	Equivalent Load Capacitance	12	18	22	pF
R _S	Series Resistance(ESR)	-	25	50	Ω
	Duty Cycle	30	50	70	%
C _i	Motional Capacitance	-	4.72	-	fF
C _{SHUT}	Shunt Capacitance	5	6.5	7.5	pF
R _i	Insulation resistor	500 MΩ Minimum at D.C.100V			

The 32768Hz frequency is used for low frequency operation. It supplies the wake-up domain for operation in lowest power mode. The clock is provided through X32KIN. Table 5-5 lists the 32768Hz crystal specifications.

Table 5-5. 32768Hz Crystal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
1/(t _{CPMAIN})	Crystal Oscillator Frequency Range	-	32768	-	Hz
t _{ST}	Startup Time	-	-	-	ms
	Frequency Tolerance at 25 °C	-20	-	+20	ppm
	Oscillation Mode	Fundamental			-
	Maximum Change Over Temperature Range	-20	-	+20	ppm
DL	Drive Level	-	-	1.0	uW
C _L	Equivalent Load Capacitance	-	18	-	pF
R _S	Series Resistance(ESR)	-	-	70	KΩ
	Duty Cycle	30	50	70	%

C_i	Motional Capacitance	-	2	-	fF
C_{SHUT}	Shunt Capacitance	-	1.1	-	pF
R_i	Insulation resistor	500 M Ω Minimum at D.C.100V			

5.5. External Memory AC Electrical Characteristics

5.5.1. Nand Flash AC Electrical Characteristics

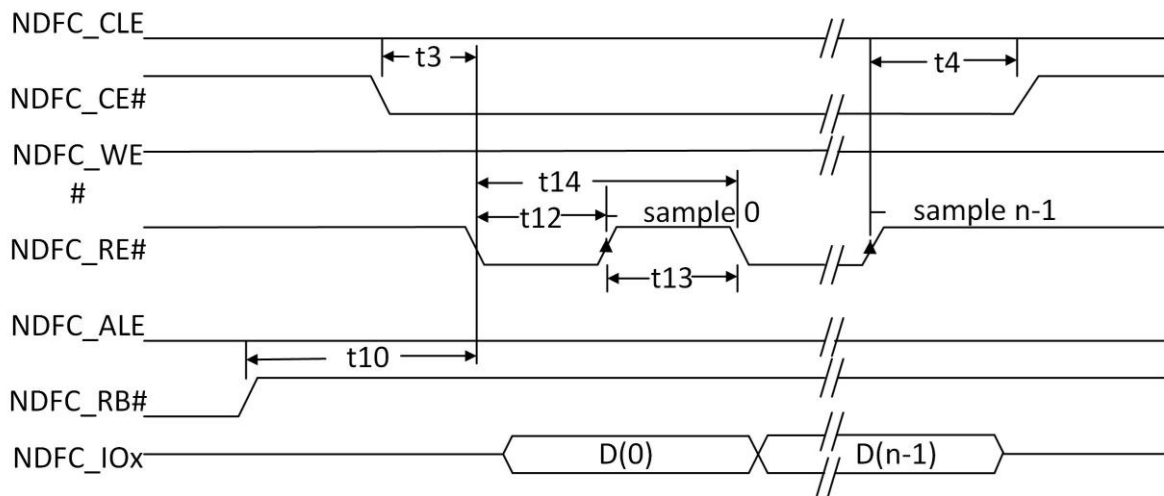


Figure 5-1. Conventional Serial Access Cycle Timing (SAM0)

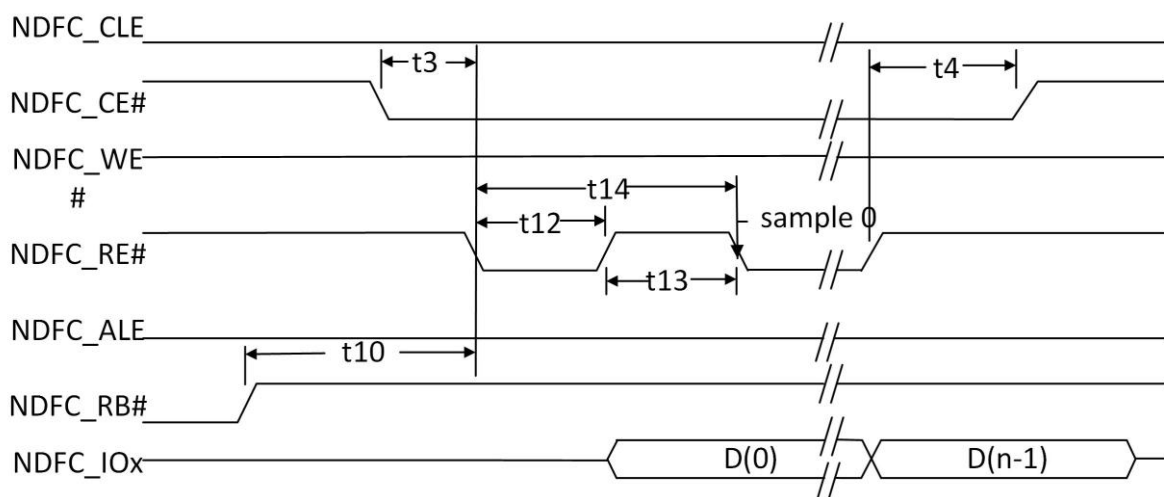


Figure 5-2. EDO Type Serial Access after Read Cycle Timing (SAM1)

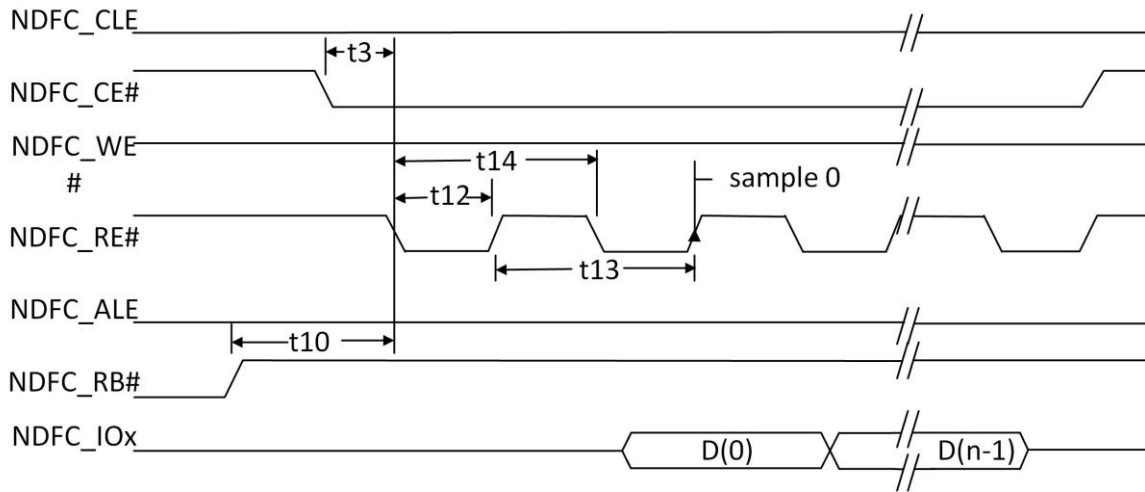


Figure 5-3. Extending EDO Type Serial Access Mode Timing (SAM2)

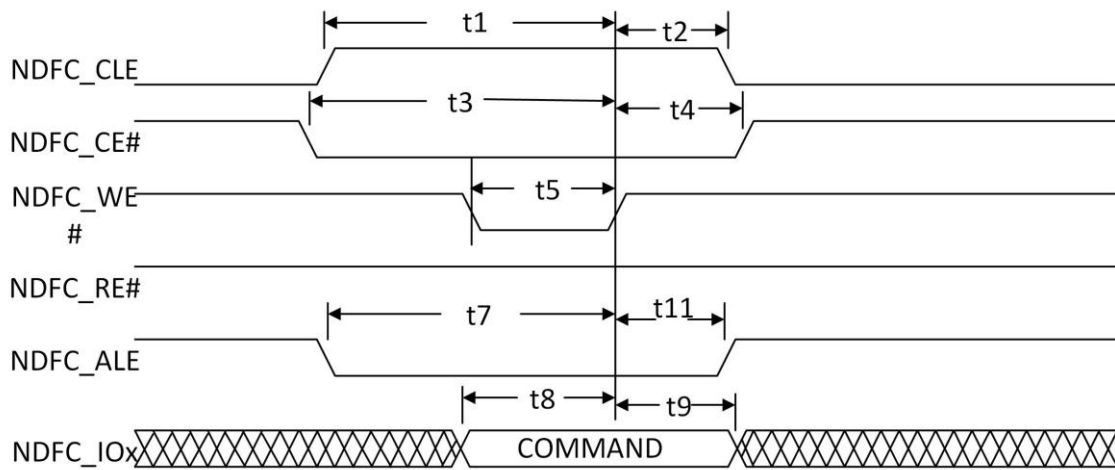


Figure 5-4. Command Latch Cycle Timing

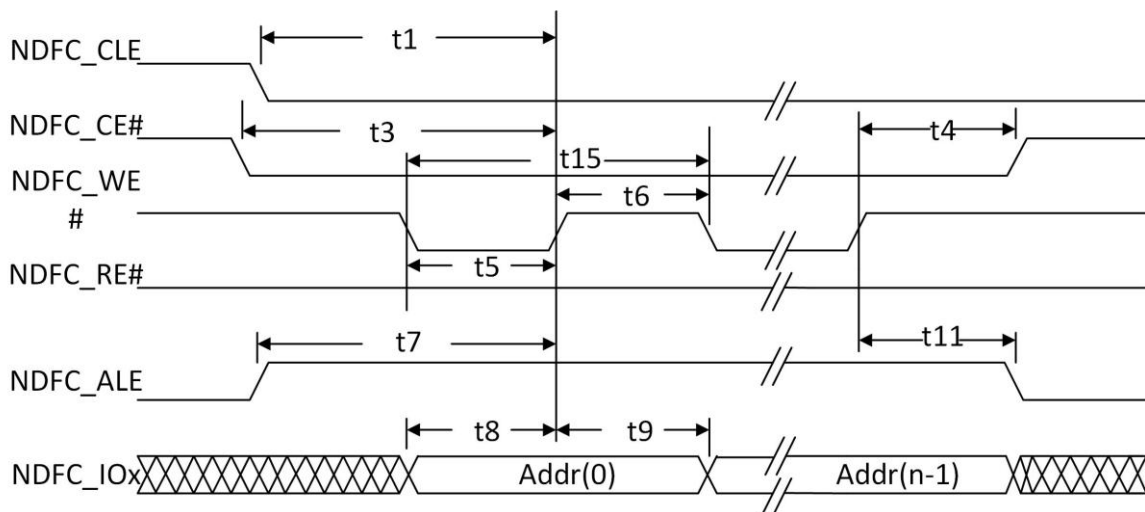


Figure 5-5. Address Latch Cycle Timing

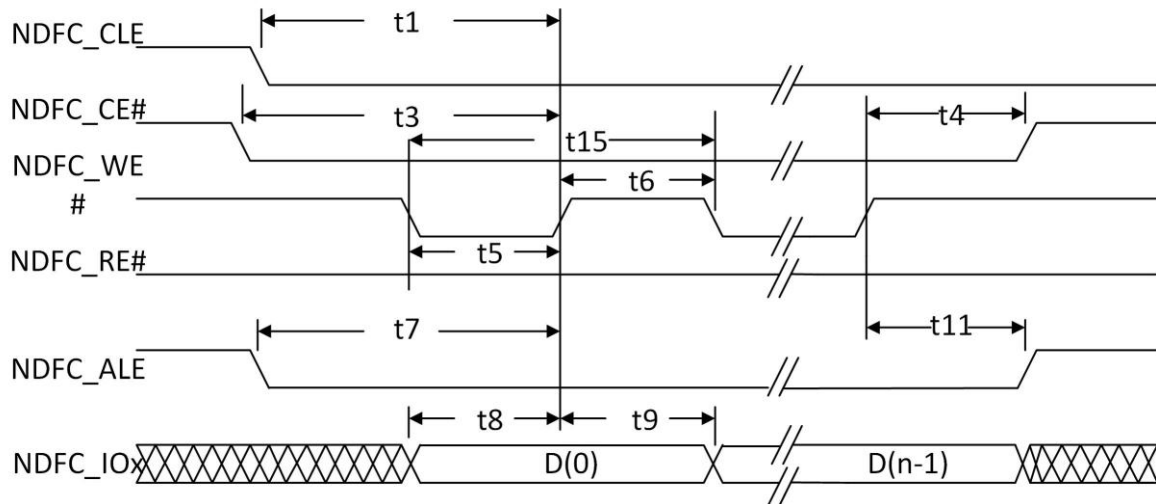


Figure 5-6. Write Data to Flash Cycle Timing

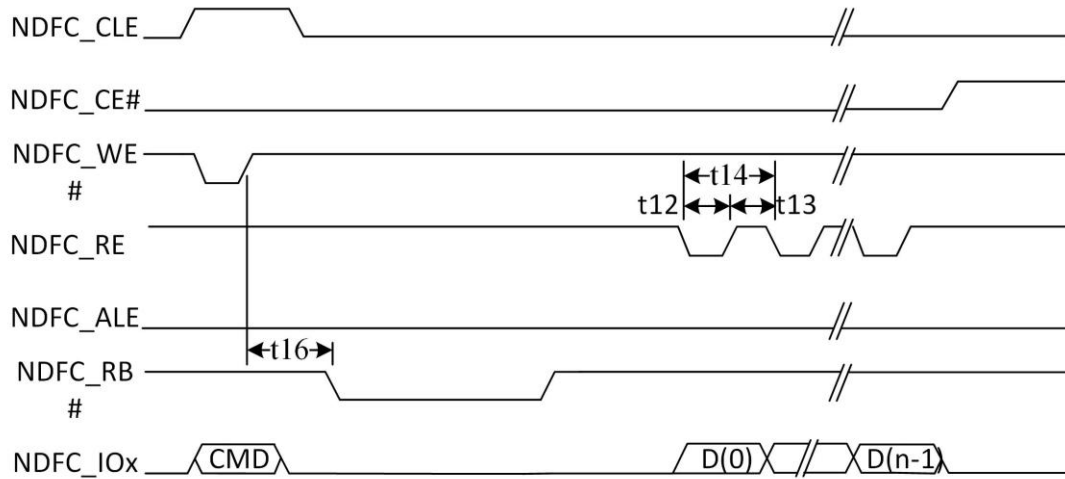


Figure 5-7. Waiting R/B# Ready Timing

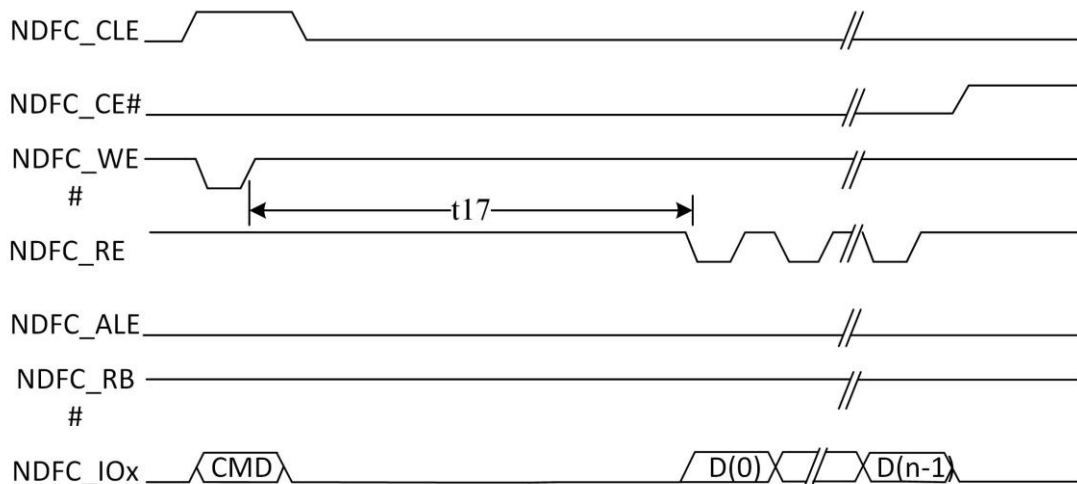


Figure 5-8. WE# High to RE# Low Timing

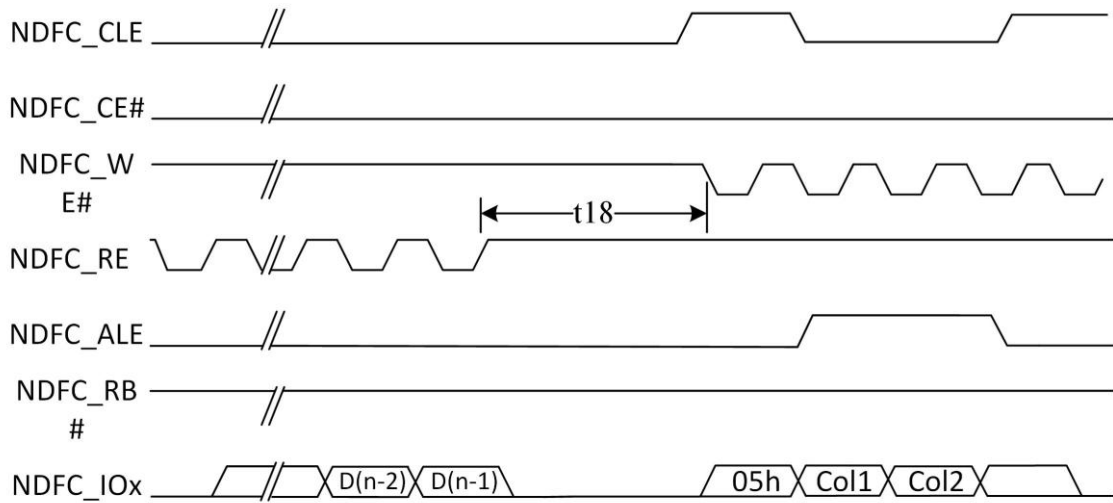


Figure 5-9. RE# High to WE# Low Timing

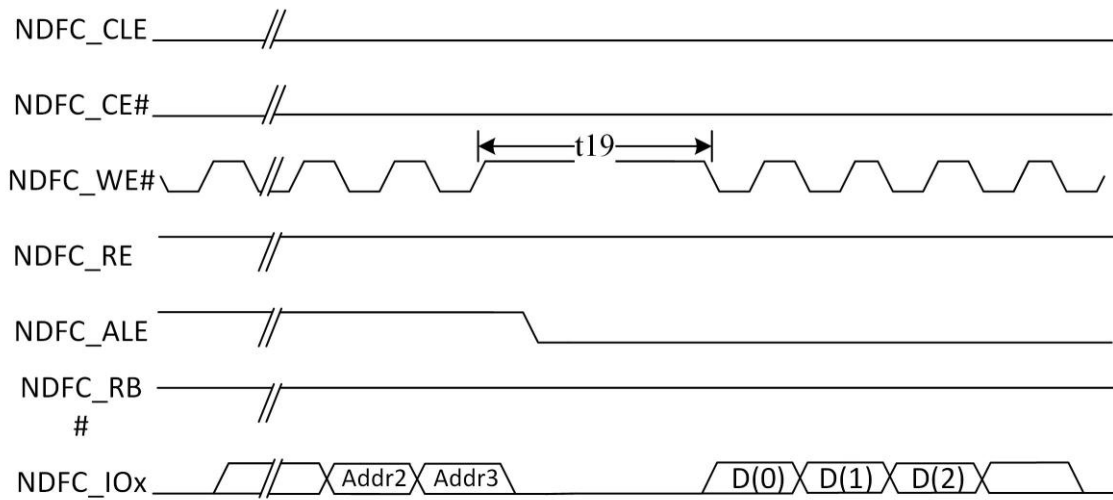


Figure 5-10. Address to Data Loading Timing

Table 5-6. NAND Timing Constants

Parameter	Symbol	Timing	Unit
NDFC_CLE setup time	t1	2T	ns
NDFC_CLE hold time	t2	2T	ns
NDFC_CE setup time	t3	2T	ns
NDFC_CE hold time	t4	2T	ns
NDFC_WE# pulse width	t5	T ⁽¹⁾	ns
NDFC_WE# hold time	t6	T	ns
NDFC_ALE setup time	t7	2T	ns
Data setup time	t8	T	ns
Data hold time	t9	T	ns

Ready to NDFC_RE# low	t10	3T	ns
NDFC_ALE hold time	t11	2T	ns
NDFC_RE# pulse width	t12	T	ns
NDFC_RE# hold time	t13	T	ns
Read cycle time	t14	2T	ns
Write cycle time	t15	2T	ns
NDFC_WE# high to R/B# busy	t16	T_WB ⁽²⁾	ns
NDFC_WE# high to NDFC_RE# low	t17	T_WHR ⁽³⁾	ns
NDFC_RE# high to NDFC_WE# low	t18	T_RHW ⁽⁴⁾	ns
Address to Data Loading time	t19	T_ADL ⁽⁵⁾	ns

NOTE(1):T is the cycle of internal clock.

(2),(3),(4),(5):This values is configurable in nand flash controller. The value of T_WB could be 14*2T/22*2T/30*2T/38*2T, the value of T_WHR could be 0*2T/6*2T/14*2T/22*2T, the value of T_RHW could be 4*2T/12*2T/20*2T/28*2T, the value of T_ADL could be 0*2T/6*2T/14*2T/22*2T.

5.5.2. SMHC AC Electrical Characteristics

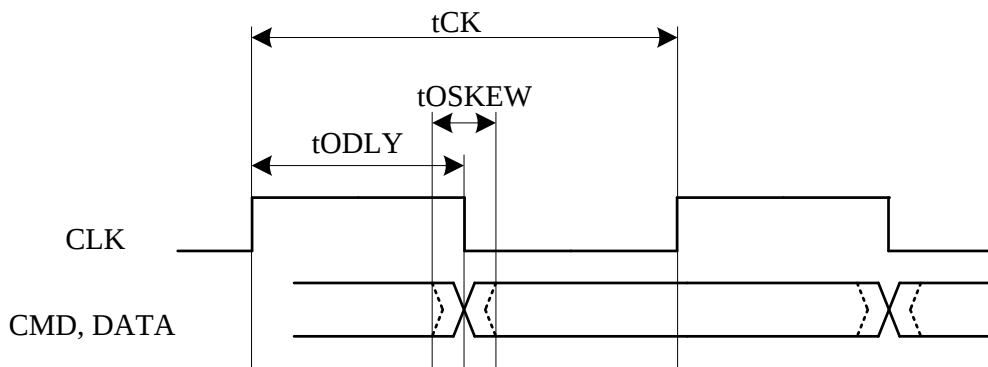


Figure 5-11. SMHC Output Timing Diagram in HS-SDR Mode

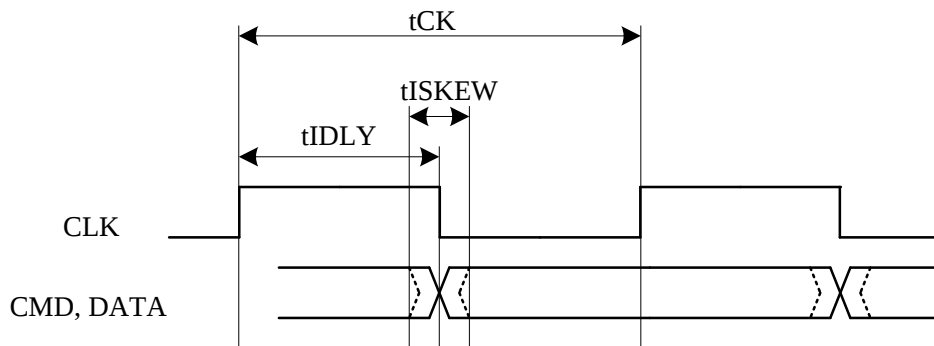


Figure 5-12. SMHC Input Timing Diagram in HS-SDR Mode

Table 5-7. SMHC Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
-----------	--------	-----	-----	-----	------	--------

Clock frequency	tCK	0	50	50	MHz	
Duty Cycle	DC	45	50	55	%	
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
Data output delay skew time	tOSKEW	-	-		ns	
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-		ns	
Data input skew time in SDR mode	tISKEW	-	-		ns	
Output CMD, DATA is referenced to CLK.						

5.6. External Peripheral AC Electrical Characteristics

5.6.1. LCD AC Electrical Characteristics

Vertical Timing

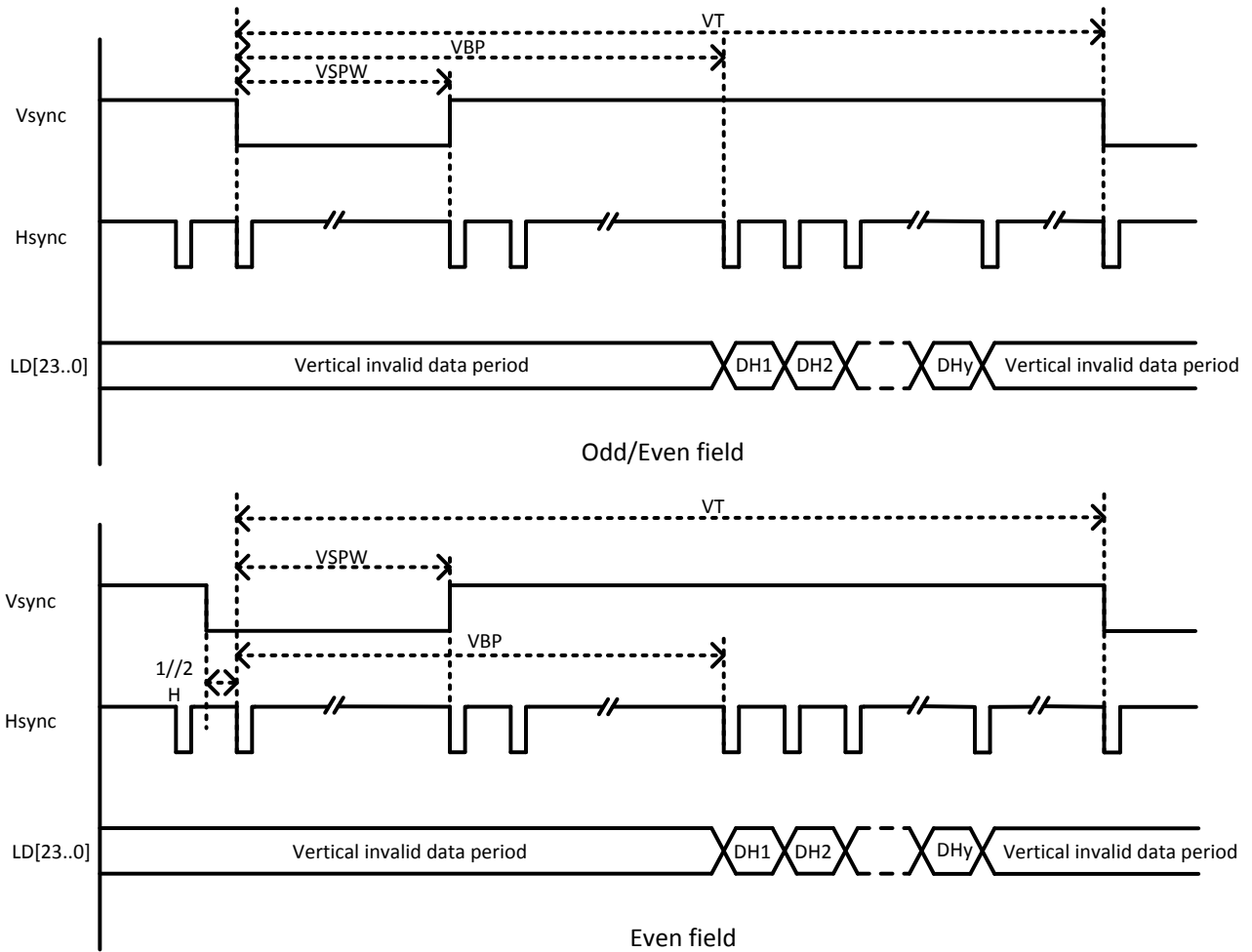


Figure 5-13. HV_IF Interface Vertical Timing

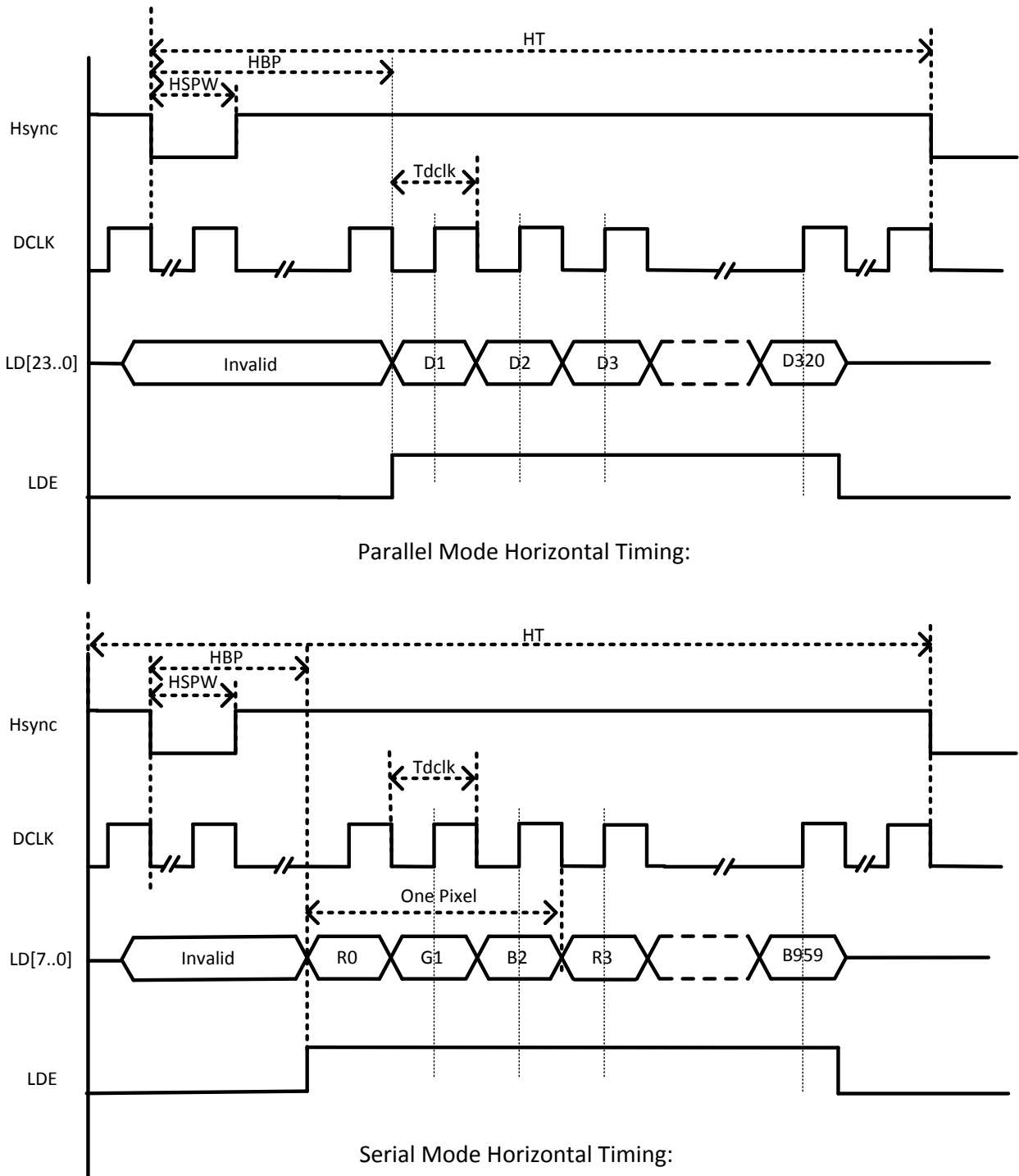


Figure 5-14. HV Interface Parallel Mode Horizontal Timing

Table 5-8. LCD HV_IF Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK cycle time	tDCLK	5	-	-	ns
HSYNC period time	tHT	-	HT+1	-	tDCLK
HSYNC width	tHSPW	-	HSPW+1	-	tDCLK

HSYNC back porch	tHBP	-	HBP+1	-	tDCLK
VSYNC period time	tVT	-	VT/2	-	tHT
VSYNC width	tVSPW	-	VSPW+1	-	tHT
VSYNC back porch	tVBP	-	VBP+1	-	tHT

Vsync: Vertical sync, indicates one new frame
Hsync: Horizontal sync, indicate one new scan line
DCLK: Dot clock, pixel data are sync by this clock
LDE: LCD data enable
LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel

5.6.2. CSI AC Electrical Characteristics

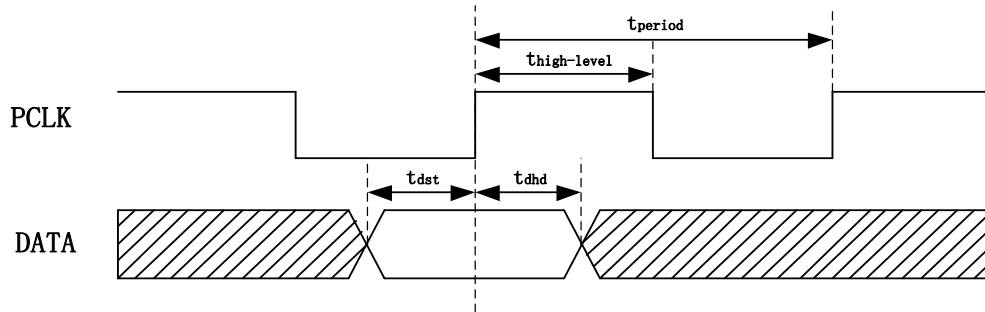


Figure 5-15. Data Sample Timing

Table 5-9. CSI Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Pclk period	t_{period}	6.67	-	-	ns
Pclk frequency	$1/t_{period}$	-	-	150	MHz
Pclk duty	$t_{high-level}/t_{period}$	40	50	60	%
Data input setup time	t_{dst}	0.6	-	-	ns
Data input hold time	t_{dhd}	0.6	-	-	ns

5.6.3. EMAC AC Electrical Characteristics

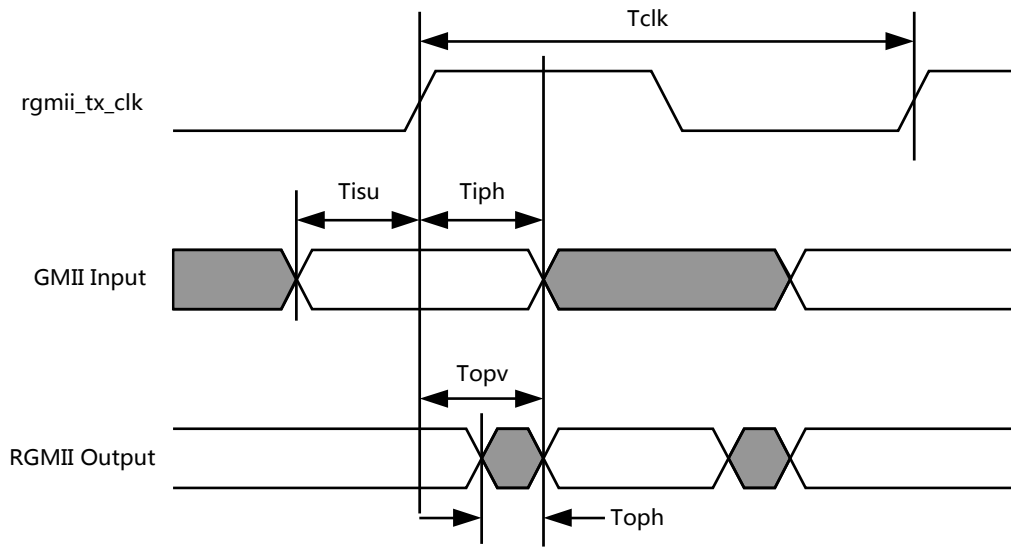


Figure 5-16. RGMII Interface Transmit Timing

Table 5-10. RGMII Transmit Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Tclk	rgmii_tx_clk clock period	8	-	DC	ns
Tisu	RGMII/TBI input set up prior to rgmii_tx_clk	2.8	-	-	ns
Tiph	RGMII/TBI input data hold after rgmii_tx_clk	0.1	-	-	ns
Topv	RGMII output data valid after rgmii_tx_clk	-	-	0.85	ns
Toph	RGMII output data hold after rgmii_tx_clk	0	-	-	ns

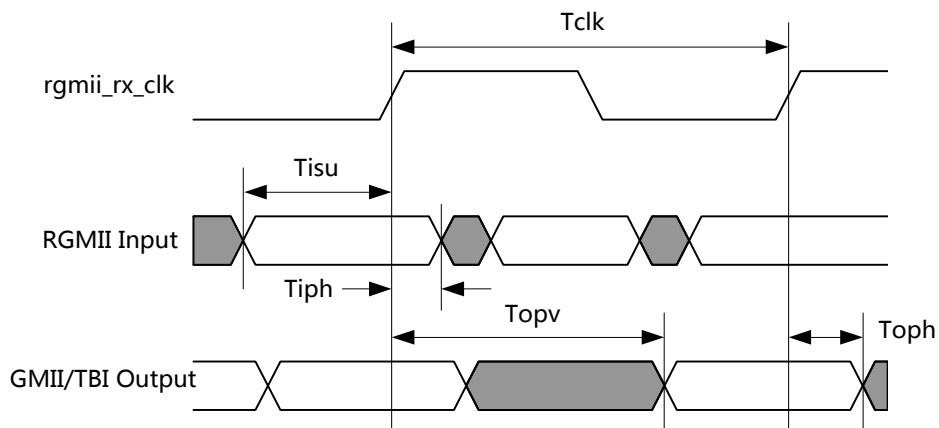


Figure 5-17. RGMII Interface Receive Timing

Table 5-11. RGMII Interface Receive Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Tclk	rgmii_rx_clk clock period	8		DC	ns
Tisu	RGMII input set up prior to rgmii_rx_clk	2.6		-	ns
Tiph	RGMII input data hold after rgmii_rx_clk	0.8		-	ns
Topv	GMII/TBI iutput data valid after rgmii_rx_clk	-		5.2	ns
Toph	GMII output data hold after rgmii_rx_clk	0.1		-	ns
	TBI output data hold after rgmii_rx_clk	0.5		-	ns

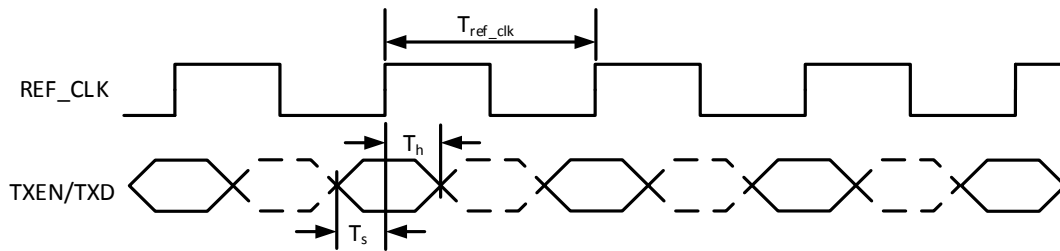


Figure 5-18. RMII Interface Transmit Timing

Table 5-12. RMII Interface Transmit Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
T _{ref_clk}	Reference Clock Period	-	20	-	ns
T _s	TXD/TXEN to REF_CLK setup time	4			ns
T _h	TXD/TXEN to REF_CLK hold time	2			ns

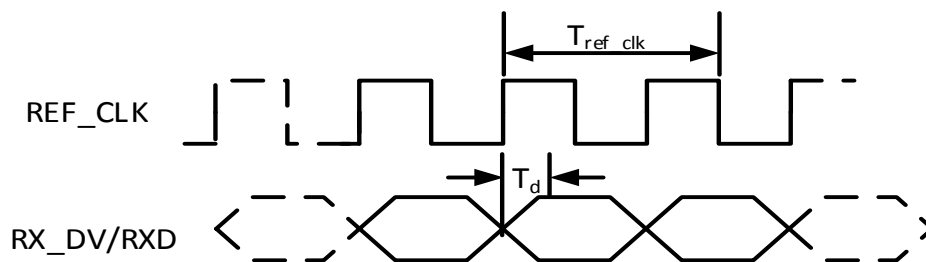


Figure 5-19. RMII Interface Receive Timing

Table 5-13. RMII Interface Receive Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
T _{ref_clk}	Reference Clock Period	-	20	-	ns
T _d	REF_CLK rising edge to RX_DV/RXD	-	10	12	ns

5.6.4. CIR Receiver AC Electrical Characteristics

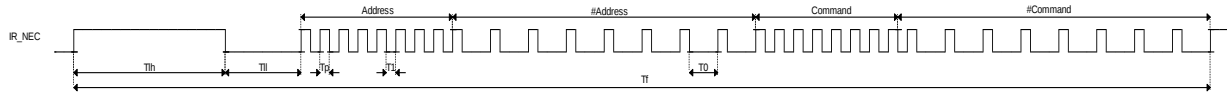


Figure 5-20. CIR Receiver Timing

Table 5-14. CIR Receiver Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Frame period	Tf	-	67.5	-	ms
Lead code high time	Tlh	-	9	-	ms
Lead code low time	Tll	-	4.5	-	ms
Pulse time	Tp	-	560	-	us
Logical 1 low time	T1	-	1680	-	us
Logical 0 low time	T0	-	560	-	us

5.6.5. SPI AC Electrical Characteristics

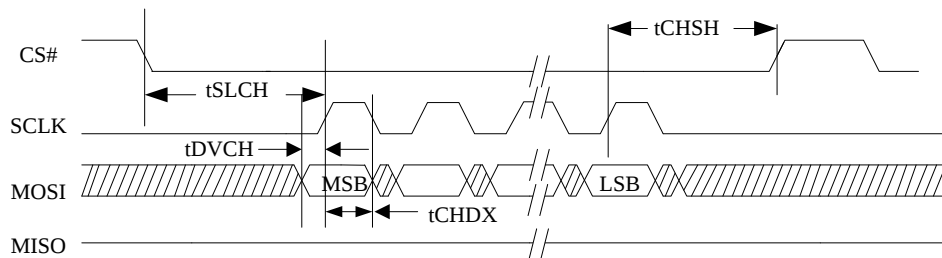


Figure 5-21. SPI MOSI Timing

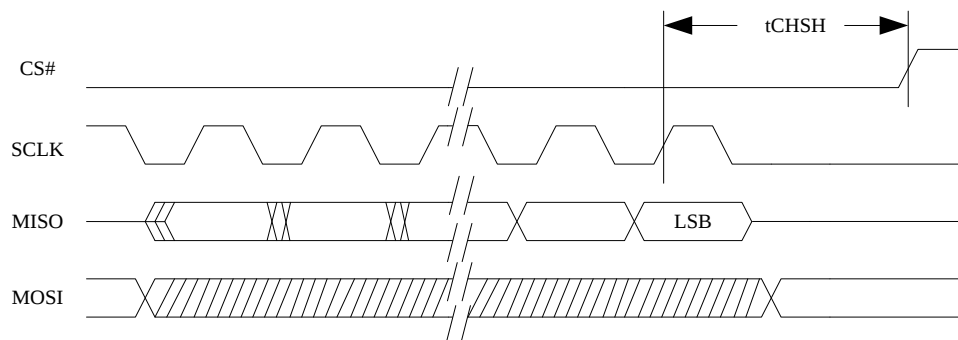


Figure 5-22. SPI MISO Timing

Table 5-15. SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# active setup time	tSLCH	-	2T	-	ns
CS# active hold time	tCHSH	-	2T ⁽¹⁾	-	ns
Data in setup time	tDVCH	-	T/2-3	-	ns
Data in hold time	tCHDX	-	T/2-3	-	ns
(1): T is the cycle of clock.					

5.6.6. UART AC Electrical Characteristics

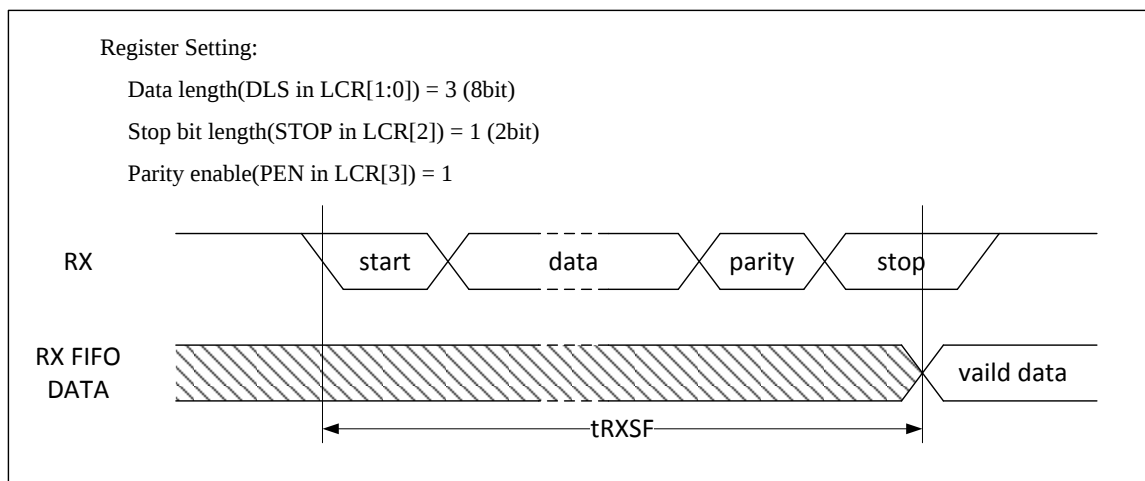


Figure 5-23. UART RX Timing

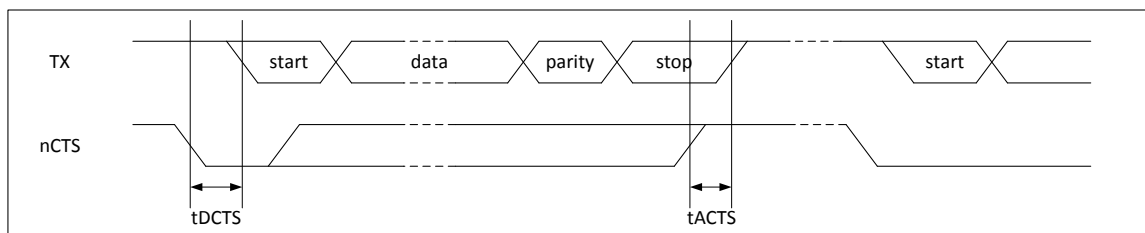


Figure 5-24. UART nCTS Timing

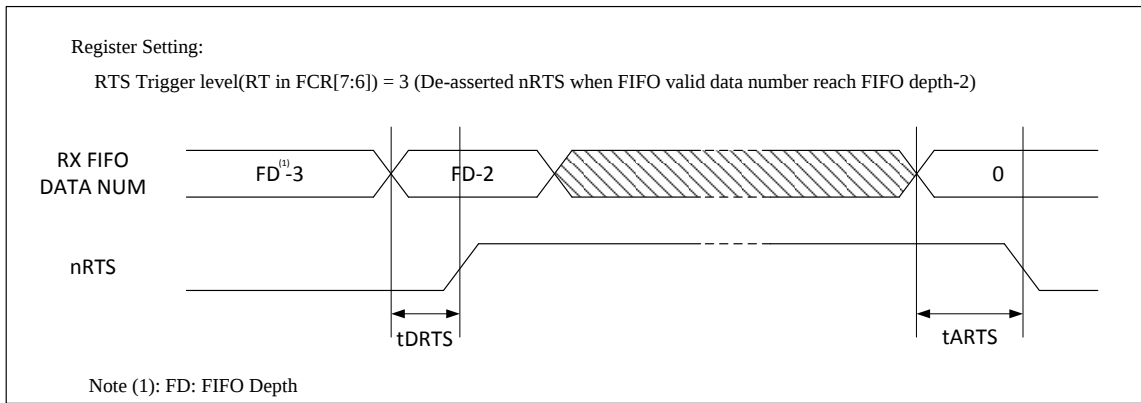


Figure 5-25. UART nRTS Timing

Table 5-16. UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	$10.5 \times \text{BRP}^{(1)}$	-	$11 \times \text{BRP}^{(1)}$	ns
Delay time of de-asserted nCTS to TX start	tDCTS	-	-	$\text{BRP}^{(1)}$	ns
Step time of asserted nCTS to stop next transmission	tACTS	$\text{BRP}^{(1)}/4$	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	$\text{BRP}^{(1)}$	ns
Delay time of asserted nRTS	tARTS	-	-	$\text{BRP}^{(1)}$	ns

(1): BRP(Baud-Rate Period).

5.6.7. TWI AC Electrical Characteristics

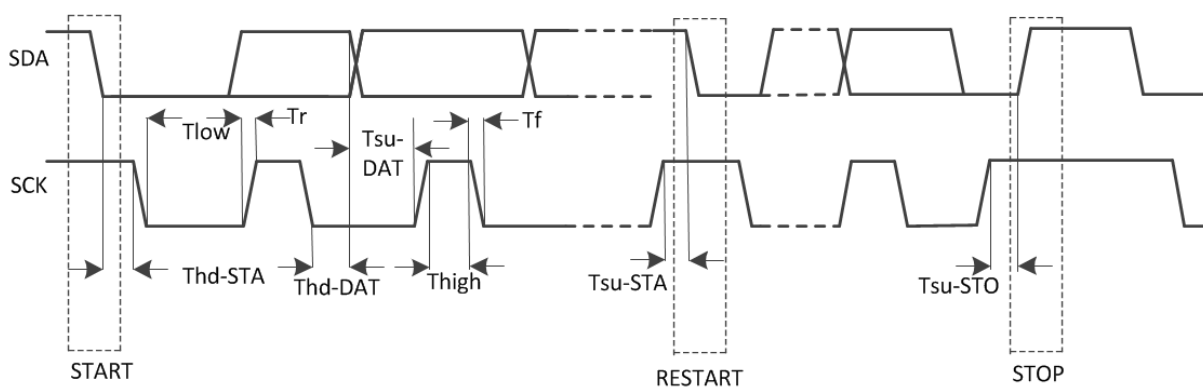


Figure 5-26. TWI Timing

Table 5-17. TWI Timing Constants

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz
Setup Time In Start	Tsu-STA	4.7	-	0.6	-	us
Hold Time In Start	Thd-STA	4.0	-	0.6	-	us
Setup Time In Data	Tsu-DAT	250	-	100	-	ns
Hold Time In Data	Thd-DAT	5.0	-	-	-	ns
Setup Time In Stop	Tsu-STO	4.0	-	6.0	-	us
SCK Low level Time	Tlow	4.7	-	1.3	-	us
SCK High level Time	Thigh	4.0	-	0.6	-	ns
SCK/SDA Falling Time	Tf	-	300	20	300	ns
SCK/SDA Rising Time	Tr	-	1000	20	300	ns

5.6.8. TSC AC Electrical Characteristics

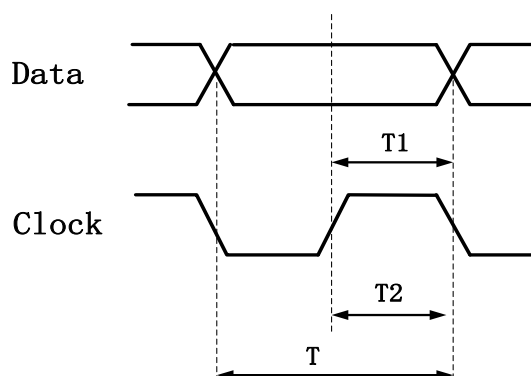


Figure 5-27. TSC Data and Clock Timing

Table 5-18. TSC Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Data hold time	T1	$T/2 - T/10$	$T^{(1)}/2$	$T/2 + T/10$	us
Clock pulse width	T2	$T/2 - T/10$	$T/2$	$T/2 + T/10$	us

(1): T is the cycle of clock.

5.6.9. SCR AC Electrical Characteristics

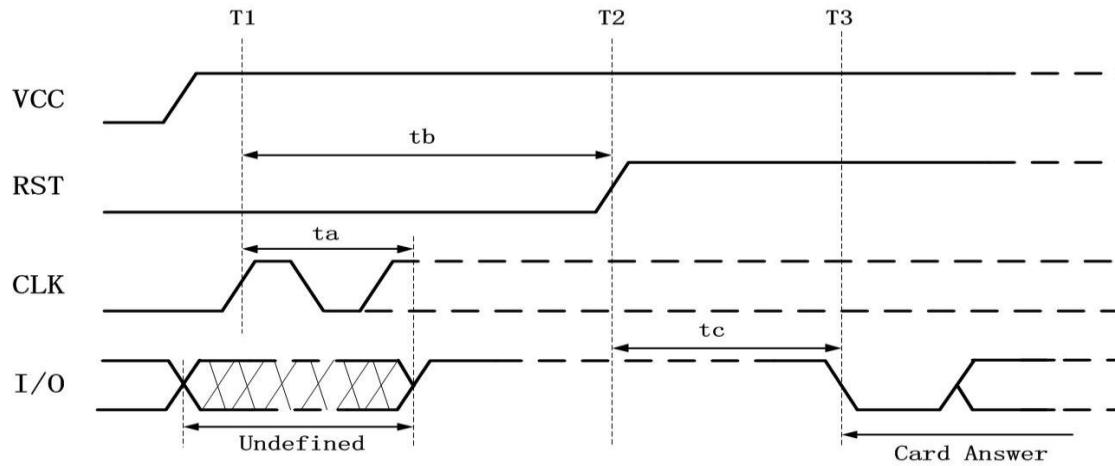


Figure 5-28. SCR Cold Reset Timing

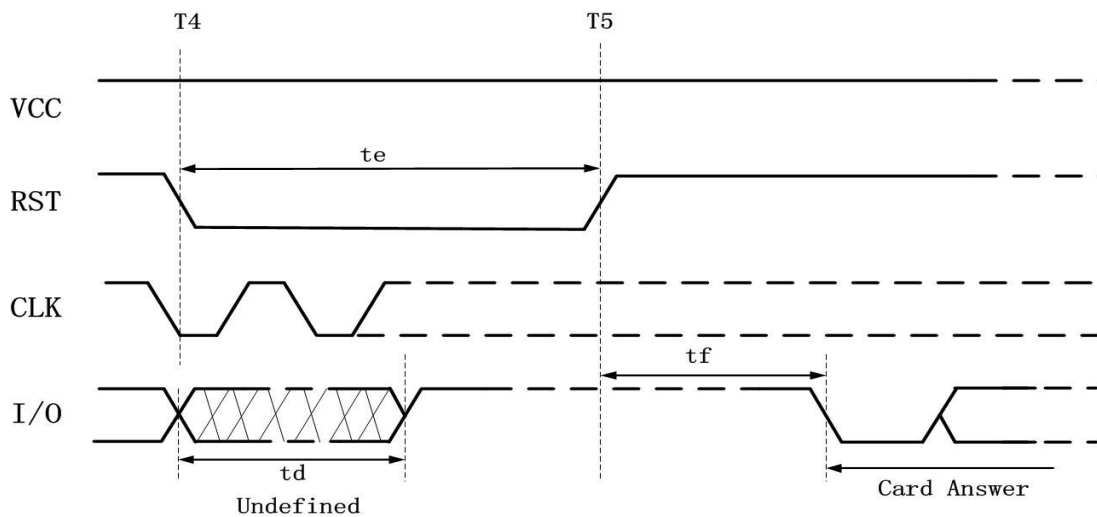


Figure 5-29. SCR Warm Reset Timing

Table 5-19. SCR Timing Constants

Symbol	Min	Typ	Max	Unit
ta	-	-	200/f	Tclk
tb	400/f	-	-	Tclk
tc	400/f	-	40000/f	Tclk
td	-	-	200/f	Tclk
te	400/f	-	-	Tclk
tf	400/f	-	40000/f	Tclk

- (1). Activation: Before time T1.
- (2). Cold Reset: After time T1.
- (3). T1: The clock signal is applied to CLK at time T1.
- (4). T2: The RST is put to state H.

- (5). T3: The card begin answer at time T3.
- (6). ta: The card shall set I/O to state H within 200 clock cycles (delay ta) after the clock signal is applied to CLK (at time T1+ta).
- (7). tb: The cold reset results from maintaining RST at state L for at least 400 clock cycles (delay tb) after the clock signal is applied to CLK (at time T1+tb).
- (8). tc: The answer on I/O shall begin between 400 and 40000 clock cycles (delay tc) after the rising edge of the signal on RST (at time T2+tc).
- (9). td: The card shall set I/O to state H within 200 clock cycles (delay td) after state L is applied to RST (at time T4+td).
- (10). te: The controller initiates a warm reset (at time T4) by putting RST to state L for at least 400 clock cycles (delay te) while VCC remains powered and CLK provided with a suitable and stabled clock signal.
- (11). tf: The card answer on I/O shall begin between 400 and 40000 clock cycles (delay tf) after the rising edge of the signal on RST (at time T5+tf).
- (12). f is the frequency of clock.

5.6.10. I2S/PCM AC Electrical Characteristics

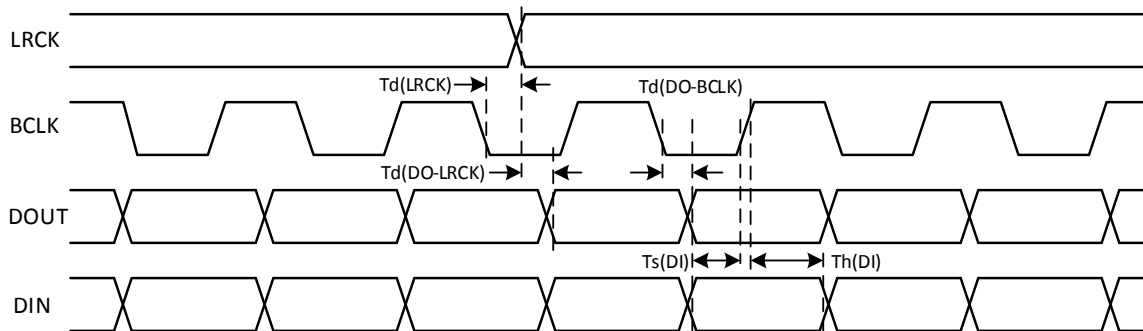


Figure 5-30. I2S/PCM Timing in Master Mode

Table 5-20. I2S/PCM Timing Constants in Master Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK Delay	$T_d(LRCK)$			10	ns
LRCK to DOUT Delay(For LJF)	$T_d(DO-LRCK)$			10	ns
BCLK to DOUT Delay	$T_d(DO-BCLK)$			10	ns
DIN Setup	$T_s(DI)$	4			ns
DIN Hold	$T_h(DI)$	4			ns
BCLK Rise Time	T_r			8	ns
BCLK Fall Time	T_f			8	ns

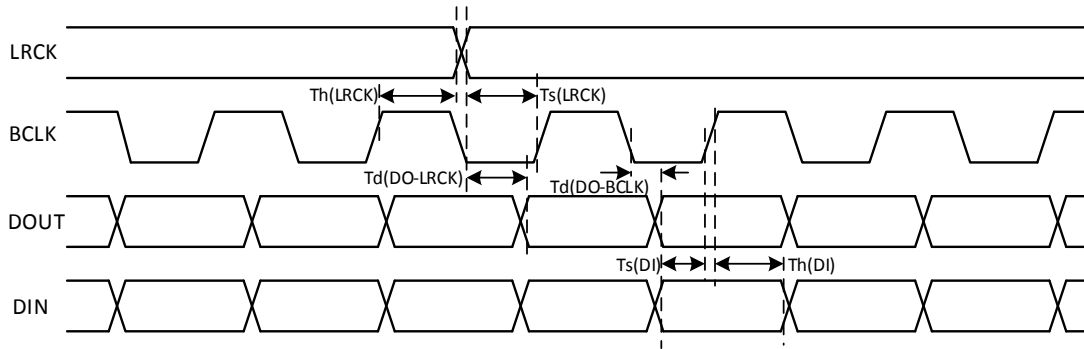


Figure 5-31. I2S/PCM Timing in Slave Mode

Table 5-21. I2S/PCM Timing Constants in Slave Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK Setup	$T_s(\text{LRCK})$	4			ns
LRCK Hold	$T_h(\text{LRCK})$	4			ns
LRCK to DOUT Delay(For LJF)	$T_d(\text{DO-LRCK})$			10	ns
BCLK to DOUT Delay	$T_d(\text{DO-BCLK})$			10	ns
DIN Setup	$T_s(\text{DI})$	4			ns
DIN Hold	$T_h(\text{DI})$	4			ns
BCLK Rise Time	T_r			4	ns
BCLK Fall Time	T_f			4	ns

5.6.11. DMIC AC Electrical Characteristics

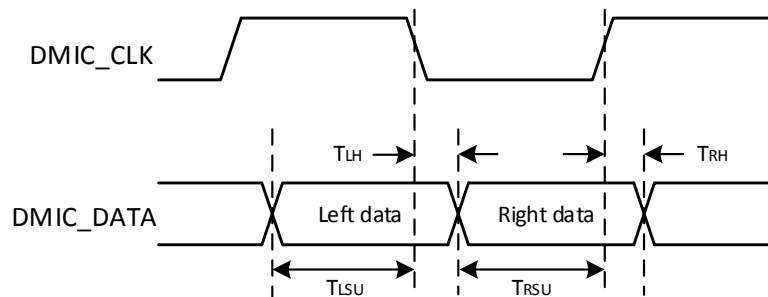


Figure 5-32. DMIC Timing

Table 5-22. DMIC Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DMIC_DATA(Left) setup time to falling DMIC_CLK edge	T_{LSU}	15			ns
DMIC_DATA(Left) hold time from falling DMIC_CLK edge	T_{LH}	0			ns
DMIC_DATA(Right) setup time to rising	T_{RSU}	15			ns

DMIC_CLK edge					
DMIC_DATA(Right) hold time from rising DMIC_CLK edge	T_{RH}	0			ns

5.6.12. OWA AC Electrical Characteristics

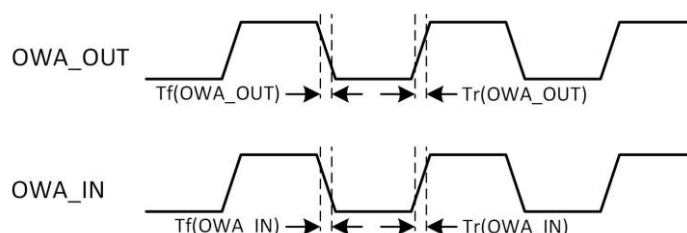


Figure 5-33. OWA Timing

Table 5-23. OWA Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
OWA_OUT Rise Time	$T_r(OWA_OUT)$			8	ns
OWA_OUT Fall Time	$T_f(OWA_OUT)$			8	ns
OWA_IN Rise Time	$T_r(OWA_IN)$			4	ns
OWA_IN Fall Time	$T_f(OWA_IN)$			4	ns

5.7. Power-up and Power-down Sequence

Figure 5-34 shows an example of the power-up sequence for H6 V200 device. The description of the power-up sequence follows.

- (1) The consequent steps in power on sequence should not start before the previous step supplies have been stabilized within 90~110% of their nominal voltage, unless stated otherwise.
- (2) VCC-RTC should remain powered on continuously, to maintain internal real-time clock status. And it has to be powered on together with VDD-CPUS, or preceding VDD-CPUS.
- (3) VDD-CPUS should be powered on together, or any time after VCC-RTC.
- (4) 32KHz clock need to start oscillating and be stable.
- (5) VDD-SYS and VDD-CPUS start to ramp simultaneously.
- (6) Other power domains can ramp after VDD-SYS and VDD-CPUS ramped.
- (7) During the entire power-up sequence, the RESET pin must be held on low until all power domains are stable.
- (8) DXVCCIO and AC-AVCC can ramp during other power supplies(such as VCC-DRAM,VCC-USB) ramp, or ramp depending on UBOOT time and BOOT time.

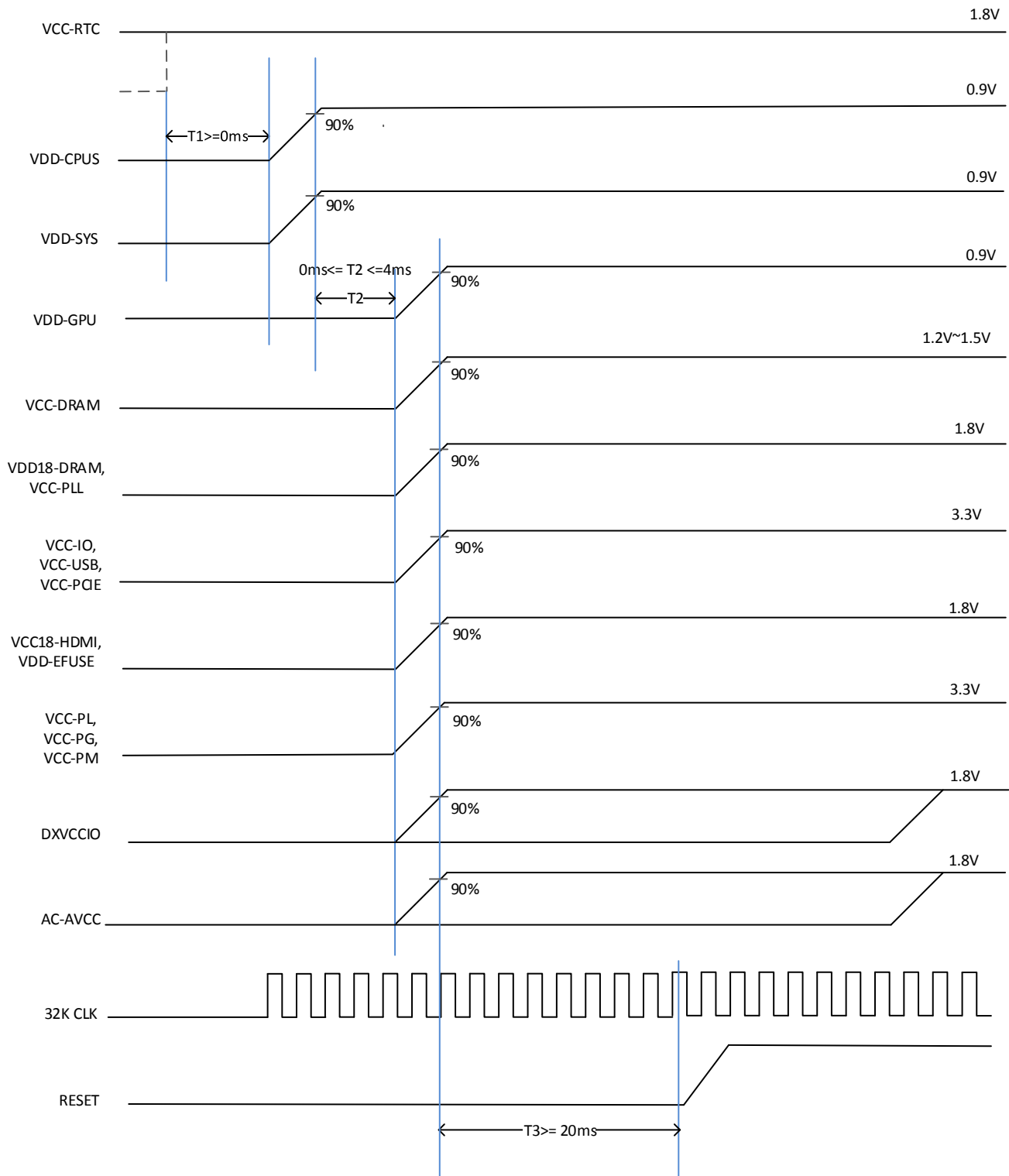


Figure 5-34. Power On Sequence

Figure 5-35 shows an example of the power-down sequence for H6 V200 device.

- (1) VCC-RTC holds high always.
- (2) After PMIC receives the power-down command, pull-down RESET#, and delay T4.
- (3) Other power start to ramp down simultaneously. The ramping down rate of each power is decided by the load on

that power supply.

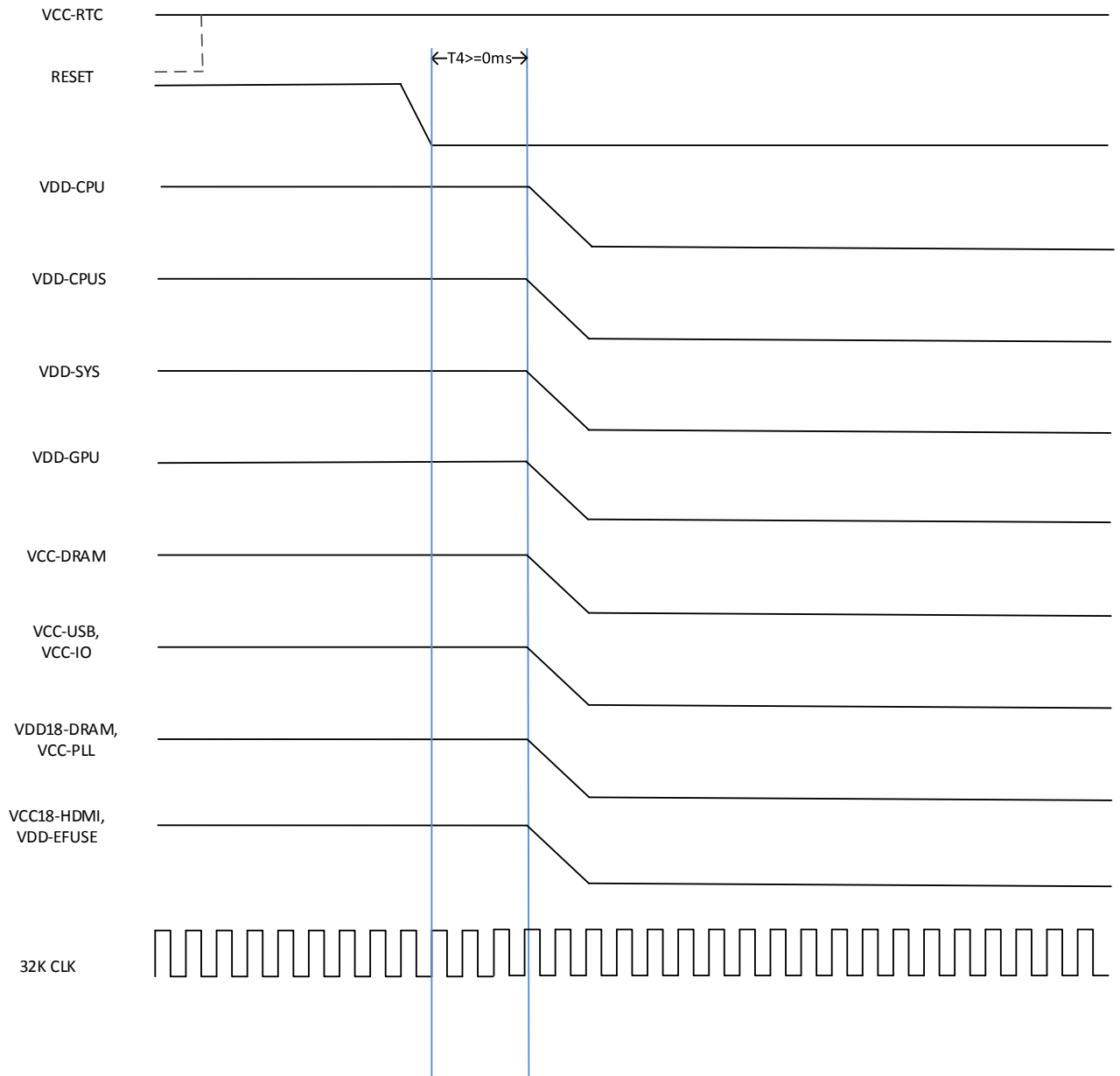


Figure 5-35. H6 V200 Power Down Sequence

5.8. Package Thermal Characteristics

Table 5-24 shows temperature and thermal resistance parameters of H6 V200. The following thermal resistance characteristics in Table 5-24 is based on JEDEC JESD51 standard, because the actual system design and temperature could be different with JEDEC JESD51 , the simulating result data is a reference only, please prevail in the actual application condition test.

**NOTE**

Test Condition: Four-layer board(2s2p), Natural Convection, No Air flow

Table 5-24. H6 V200 Thermal Resistance Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-20	-	+70	°C
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	23.1	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	11.97	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	8.07	-	°C/W

Appendix

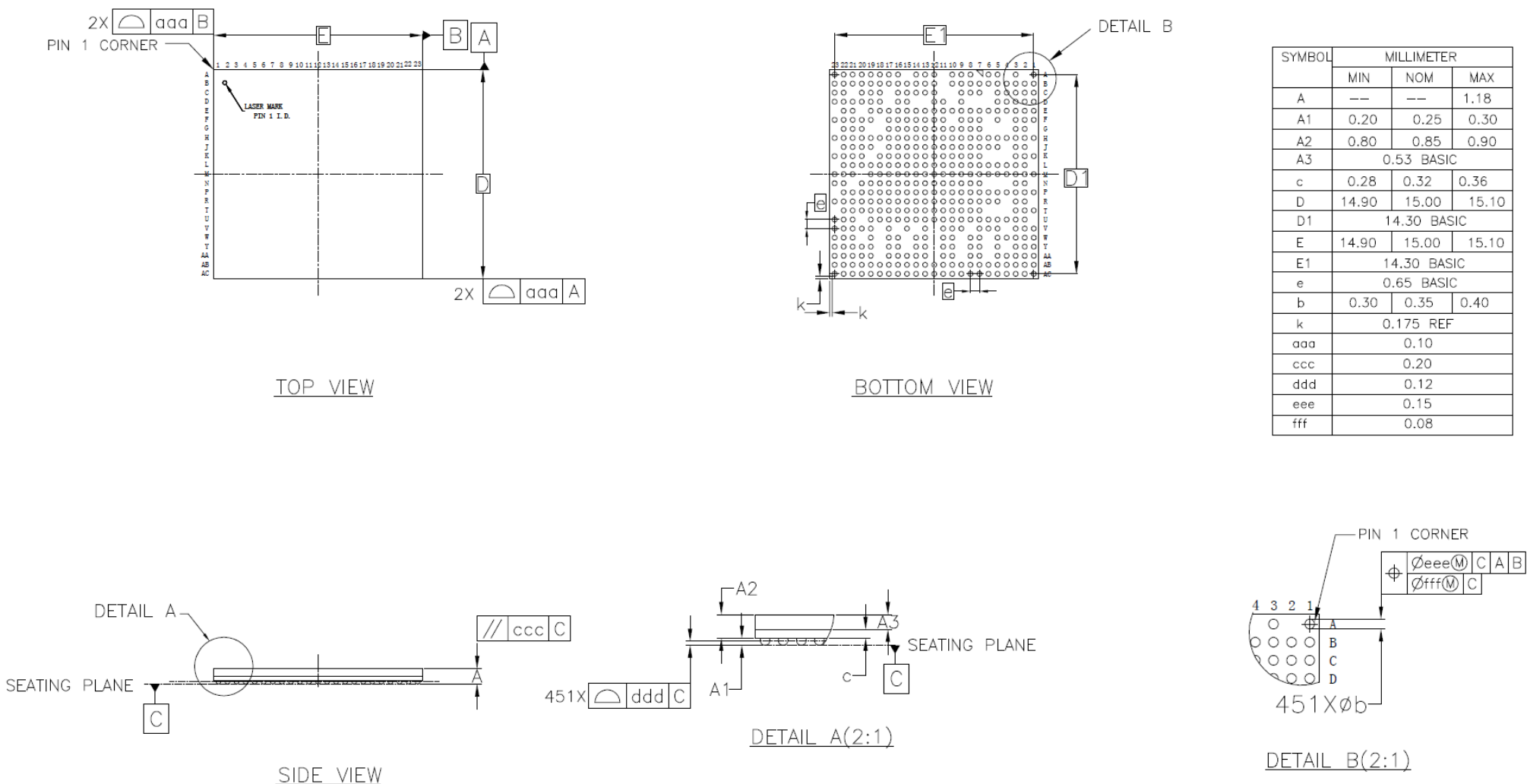
Pin Map

The following figure shows the pin maps of the 451-pin FBGA package of H6 V200 processor.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A	AGND		TV-OUT		EPHY-TXP	EPHY-RXP		PCIE-REF-CLKP	PCIE-TXP	PCIE-RXP		USB2-DM	USB0-DM	USB1-SSRXN		GND	HTX2P	HTX1P	HTX0P	HTXCP	GND	DXVCCIO	GND
B	MIC2P	MIC2N	VCC-EPHY	EPHY-RTX	EPHY-TXN	EPHY-RXN	EPHY-LNK-LED	PCIE-REF-CLKM	PCIE-TXM	PCIE-RXM		USB2-DP	USB0-DP	USB1-SSRXP	USB1-SSTXN	USB1-DM	HTX2N	HTX1N	HTX0N	HTXCN	NC	DXOUT	DXIN
C	MIC1P	MIC1N	VCC-TV	VRA1	EPHY-SPD-LED		TEST2	PF6	PH0			GND	GND	GND	USB1-SSTXP	USB1-DP		GND	VCC18-HDMI	HHPD		GND	REFCLK_OUT
D	LINEOUTR	LINEOUTL	AC-AVCC	VRA2	AC-SYS-VDD-OUT			PH6		PH3	PH1				HSIC-STR	HSIC-VCC		VDD09-HDMI	BIAS-VRAL	BIAS-ITEST	BIAS-REXT	DXLDO_OUT	GND
E	AGND	PF0	AGND	AC-LDOIN	AGND	AC-SYS-VDD-IN	TEST3	TEST1	PH10	PH8	PH2	PH4	GND	VCC-USB	GND	GND	HSIC-DAT	GND	VCC18-BIAS		CLOCK-SELECT	WREQIN	
F	PF4	PF2	PF1		MBIAS		PH9	PH7	PH5		JTAG-SELO	GND	GND	GND	GND	GND	GND		RTC-VIO	VCC-RTC	GND	X32KOUT	X32KIN
G		PF5	PF3				GND	VCC-IO	GND	JTAG-SEL1	VDD-EFUSE	VDD09-PCIE	VDD-SYS	VDD-SYS	GND	VDD-USB	UBOOT			X32KFOUT	NMI	RESET	
H	GND	PG3	PG8	PG6	PG5	VCC-PG	GND	GND	GND	GND	VCC-PCIE	GND	VDD-SYS	VDD-SYS	GND	GND	BOOT-SELECT	VCC-PL	TEST	PL6	PL10	PL8	GND
J		PG0	PG1		PG2	PG7	GND	GND	GND	GND	GND	GND	VDD-SYS	VDD-SYS	GND	GND	GND		PL9	PL3	PL7	PL5	
K	PG9	PG11	PG10				GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD-CPUS		PL0	PL4	PL2	PL1
L		PG14	PG12	PG13	PG4	PD2	GND	VDD-GPU	GND	GND	GND	GND	GND	GND	GND	VDD-CPU	VDD-CPU	GND	PM4	PM0	PM1	PM2	
M	GND	PD4	PD1	PD5	PD3	PD10	GND	VDD-GPU	VDD-GPU	GND	GND	GND	GND	GND	GND	VDD-CPU	VDD-CPU	GND	VCC-PM		PC5	PM3	GND
N		PD6	PD0				GND	VDD-GPU	VDD-GPU	GND	GND	GND	GND	GND	GND	VDD-CPU	VDD-CPU	GND	VCC-PC	PC4		PC6	PC7
P	PD11	PD9	PD19	PD18	PD8	PD13	GND	VDD-GPU	VDD-GPU	GND	GND	GND	GND	GND	VDD-CPU	VDD-CPU	VDD-CPU	VCC-PLL	PC15	GND	PC16	PC2	
R		PD16	PD15		PD26	VCC-PD	VDD-GPUFB	GND	GND	GND	GND	GND	GND	GND	GND	VDD-CPUFB	GND	GND	PC14	PC1	PC0	PC8	PC9
T	PD7	PD17	PD21				GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD-CPUFB	GND	GND	PC3	PC11	PC10	
U		PD22	PD25	PD14	PD23	GND	GND	VCC-DRAW	GND	GND	GND	GND	VCC-DRAW	VCC-DRAW	GND	VCC-DRAW	GND	GND	PC12		PC13	GND	GND
V	PD24	PD12	PD20		GND	SVREF	GND		VCC-DRAW	VCC-DRAW	VCC-DRAW		GND		VCC-DRAW		GND		GND	GND	PLL-TEST	X24MIN	X24MOUT
W	GND	SDQ	GND	SPAR	SA13		SBA0	SBG0		GND	SBG1		SCS0	SCKE0		SA12	SA11		SCAS/SA15		GND	VDD18-DRAW	GND
Y	SDQ24	SDQ25	SA9		GND		SA17	SA6		SA5	SCKE1		GND	SCS1		SA4	SA10		GND	SA3	SALERT	SDQ15	SDQM1
AA	SDQ26	SDQ27	SRST	SRAS/SA16	SA7		SA8	GND		SODT1	SACT		SODT0	SWE/SA14	SA0	GND	SA1		SA2	SBA1	GND	SDQ14	SDQ13
AB	SDQS3P	SDQS3N	GND	SDQ31	SDQM3	SDQ17	SDQ19	SDQS2P	SDQ21	SDQ23	SDQM2	SCKN	GND	SDQ5	SDQ4	SDQS0N	SDQ2	SDQ0	SDQ8	SDQ11	GND	SDQS1N	SDQ12
AC	GND	SDQ28	SDQ29	SDQ30	GND	SDQ16	SDQ18	SDQS2N	SDQ20	SDQ22	GND	SCKP	SDQ7	SDQ6	SDQS0P	SDQ3	SDQ1	SDQM0	GND	SDQ9	SDQ10	SDQS1P	GND

Package Dimension

The following diagram shows the package dimension of H6 V200 processor, includes the top, bottom, side views and details of the 15mmx15mm package.



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Allwinner Technology Co.,Ltd.

No.9 Technology Road 2, High-Tech Zone,

Zhuhai, Guangdong Province, China

Contact US:

Service@allwinnertech.com

www.allwinnertech.com